

**Office of the Dean Research and Consultancy  
Indian Institute of Engineering Science & Technology (IEST), Shibpur  
Howrah-711 103**

**Project on: “Design and Development of WBG Device Based High Current Converters for Industry Applications”;**

**PI: Prof. Mainak Sengupta, Department of Electrical Engineering**

**[Sponsoring Authority: MeTy, Govt. of India]**

**Department of Electrical Engineering,  
Indian Institute of Engineering Science & Technology (IEST), Shibpur  
Howrah-711 103**

**Ref: Advt. No. EE 1851, published in the “Statesman (All Edition” & “Dainik Statesman (Bengali)”, dated 01.08.2024**

**[University Project Code: DRC/MEITY-NAMPET-III (WBG)/EE/MS/006/20-21]**

Interested candidates are requested to appear for a walk-in interview(s) for the following post in the Department of Electrical Engineering, Indian Institute of Engineering Science & Technology (IEST), Shibpur, Howrah-711103.

**Name of the post(s):** Senior Project Associate.

**No of post(s) –** One (01)

**Essential Qualification(s):**

1. M.E. / M. Tech or equivalent degree in Electrical Engineering from a recognized Indian University/Institute with 60% marks or 7.0 CGPA. OR
2. B.E. / B.Tech. in Electrical Engineering from a recognized Indian University/Institute with 60% marks (or 7.0 CGPA) and minimum 5 years of Industrial or R&D experience in Power Electronics and Embedded systems.

**Desirable Qualification:**

1. Persons with more years of experience in the domain of Power Electronics and Embedded systems may be given preference.
2. Knowledge of FEM based simulation of EMI/EMC and Icepack of HF-PCBs.
3. Hands on experience in Power Electronic circuit design, analysis, fabrication and testing.
4. Sound knowledge of PCB design software like Eagle, Ki-Cad
5. Sound knowledge of open source software like SEQUEL, LT Spice etc.
6. Programming knowledge in Digital Processor such as FPGA / DSP.

**Fellowship amount:** Rs. 43,400/- consolidated, as per Gol rules.

**Age Limit:** Preferably below 35 years (Upper age limit is relaxable for SC/ST/OBC/Woman and physically handicapped candidates, as per Gol norms for Govt. funded R&D projects).

**Duration:** 5 months or till the termination of the project whichever is earlier, unless notified otherwise by the funding agency.

Interested eligible candidates should mail soft copies of the application letter in plain paper, recent bio-data,. All documents should be self-attested. Physical documents, including the above and all marksheets and certificates, in original, shall be verified both before the interview and at the time of joining. The selection will be canceled if any discrepancies are found in the documents at the time of physical verification.

**Mode, Venue and Date of the interview:** (i) Walk in interview (ii) Office of the Department of Electrical Engineering, IEST Shibpur (iii) Date & Time of Interview: **21.08.2024 at 04:00 pm**

**Note:**

1. Soft copies of the application letter, bio-data, mark sheets and certificates should be sent through e-mail in advance by 14.08.2024 5:00 PM, to: Prof. Mainak Sengupta, Project Investigator (E-mail id: [msg.ee@faculty.iests.ac.in](mailto:msg.ee@faculty.iests.ac.in)) with copy to [bhaskaran.ee@faculty.iests.ac.in](mailto:bhaskaran.ee@faculty.iests.ac.in). Only candidates applying as above shall be considered for the interview on 21.08.2024.
2. No claims for TA/DA shall be entertained.
3. All applications must mention a valid e-mail id and mobile number for communicating.
4. Short listing may be done before the interview, as per rules.

**Dean (R & C)**

**(W. Code DRC-010/24-25)**