Realization of high efficiency interdigitated back-contact (IBC) silicon heterojunction (SHJ) solar cells with novel front structure

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Brief Description of the Project

This project demonstrates the feasibility of interdigitated back contact cell structure, compatible with thin silicon wafers, ensuring low thermal budget and designing the contact structure to enable simplified module assembly. This will address the broad industry need for high efficiency c-Si cell.

Keywords: Solar Cell, Silicon Heterojunction, Interdigitated back contact

Methodologies/Approaches Adopted

The objective of the present work (IBC-SHJ cell: Fabrication Methodology) is to develop complete fabrication steps that incorporate high efficiency features such as surface texturing and high quality surface passivation into a high efficiency IBC-SHJ cell. Here we describe the complete methodology in terms of activity plan.

Activity 1: Reflection reduction from the front surface

A. Conventional Micro- Texturization

Texturization of the surface of <100> c-silicon wafer by anisotropic etching is an effective means that is widely used to reduce surface reflectance and enhance light trapping in silicon solar cells. The etching process leads to the formation of <111> pyramidal structures on the silicon surface which allow light to be more easily coupled into the silicon and efficiently absorbed into the solar cell. Wafers will be pre-cleaned by using Acetone, Methanol and Isopropanol followed by Piranha (H_2O_2:H_2SO_4) treatment. Front surface texturing will be done by Tetramethyl-ammonium hydroxide (TMAH) or HNA (mixture of hydrofluoric acid and nitric acid) solution.

B. Development of anti-reflection stack

The front surface anti-reflection stack consists of Silicon nitride (a-SiNx:H) and Silicon carbide (a-SiC:H) layer will be developed. SiNx thin films have attracted great attention in silicon solar cell manufacturing due to their excellent passivation and antireflection properties. For a good anti-reflection coating a quarter wavelength optical slab of silicon nitride ontexturized silicon substrate is chosen. The slab is designed to have a quarter wavelength thickness at 550nm wavelength of light where there are maximum photons in the AM1.5G solar spectrum. SiC layer will protect SiN_x layer during different etching steps.

C. Novel Nano- Micro structures on silicon substrate

The eyes and wings of some species of moth are covered in arrays of sub-wavelength structures to reflect as little sunlight as possible. We would be investigating ways of exploiting this to reduce

reflection from the surfaces of silicon solar cells. Nano anti reflection structures would be simulated in the opto- electrical domain and optimization carried out. The experimental realization of optimized biomimetic antireflective moth-eye arrays in silicon will be done using a technique based on nanoimprint lithography and dry/ wet etching. It may be noted here that properly optimized structures will not only provide anti- reflective properties but also significant light scattering leading to enhance path length of light inside the solar cell.

Activity 2: Optimization of surface passivation layer

Crystalline silicon (c-Si) is an indirect semiconductor, and hence, recombination losses in this material occur largely via defect levels within the band gap. These defects are located within the bulk and at the surfaces of the wafer. There are extrinsic, or process-related, and intrinsic, or silicon-related, defects. These silicon related defects are unavoidable. Because of the involvement of non-silicon atoms, the situation is more complicated at the Si surface. The surface represents the largest possible disturbance of the symmetry of the crystal lattice and hence, because of non-saturated or dangling bonds, a large density of defects within the band gap exists at the surface of the crystal. There are additional process related extrinsic surface defects, for instance, due to dislocations or chemical residues and metallic deposition on the surface. To keep surface recombination losses at c-Si surfaces at tolerable levels, they must be electronically well passivated. In our study we will use hydrogenated amorphous silicon as the surface passivation layer. Surface passivation is strongly depends upon the optoelectronic properties of the amorphous layer so it needs special attention during optimization. Passivation layer will be developed using a chamber of a cluster tool PECVD system.

Activity 3: Selection and optimization of masks for lithography

It is intended to maximize the coverage of p-type a-Si/n-type c-Si junction without incurring resistive or other junction losses in n-type base fingers. Different sets of solar cells with p/n-type finger widths of 1.0 mm – 1.4 mm/0.5 mm – 0.2mm will be fabricated. Another variable indicates the width of the gap between the p- and n-contact fingers. It is intended to minimize the width of this gap to reduce recombination losses and enhance the electric field in the c-Si bulk between the p- and n-type a-Si fingers. However, close grid spacing may pose alignment challenges during high-volume manufacturing. This gap width will be set within 50 μm for fabricated solar cells. So the masks for n-strip and p-strip will be designed and fabricated accordingly.

Activity 4: Optimization of photo lithography, selection of proper photoresist and etchant

In this activity selection will be done from a variety of positive photo-resists like Shipley S-1818, S-1813, AZ4210 (IR photoresist) etc. The process parameter like etch rate, dilution, photo-resist selectivity will be done using standard etchants like BHF, ortho-phosphoric acid etc.

Activity 5: Optimization of emitter layer and back surface field (BSF)

The emitter (p-a-Si:H or p-a-SiO:H) and BSF (n-a-Si:H or n-a-SiO:H) will be optimized in different chamber of a cluster tool PECVD system having 13.56 MHz RF source. Here we will vary different process parameter like power density, chamber pressure, gas dilution, substrate temperature, inter electrode spacing for optimizing the device quality emitter and BSF. Deposited film will be characterize in detail using UV-VIS spectrophotometer, FTIR, Dark and photo conductivity etc.

Activity 6: Optimization of single or stack metal layers

Depending on the structure of the metal stack used to contact the doped areas, the reflectivity of this back reflector is considerably changed. We will deposit aluminum (Al) or silver (Ag) by E-beam/thermal evaporation system for emitter and base connection. We will also try metal stack like Al/Sb/Ti or Si/Ti/Ag which does not need any annealing and provides electrical contacts and able to improve the efficiency of an IBC (Interdigitated Back Contacts) solar cell.

Activity 7: Fabrication & characterization of complete IBC-SHJ solar cell

We will fabricate 5 cm x 5 cm area IBC-SHJ solar cell with target efficiency ~ 18% (target efficiency is competitive with global efficiency level of such IBC-SHJ solar cell, see table in International Status Review) with the structure and process steps mentioned in project outline. Fabricated cells will be characterize in detail like JV, QE.

Activity 8: Environmental degradation and stability study

Finally the cells will be exposed for environmental degradation and stability study

Project Highlights

Interdigitated-back-contact heterojunction crystalline silicon solar cells have a potential to reach very high efficiency due to the short-circuit current density and fill factor advantage of the back contact design, and the high open-circuit voltage of heterojunction structures. The highest efficiency (20.1%) modules on the market today are manufactured by Sun Power using Integrated Back Contact (IBC) solar cells but diffused junction. The open circuit voltages (680 mV) are considerably lower than Sanyo's (745 mV) silicon heterojunction (SHJ) solar cells. In our proposal we are trying to combine the advantage of both IBC and SHJ and to design high efficiency IBC-SHJ solar cells. Further, novel front antireflective nano structures would also be incorporated in the front surface to reduce the reflection losses leading to an increase in overall efficiency of the solar cell.

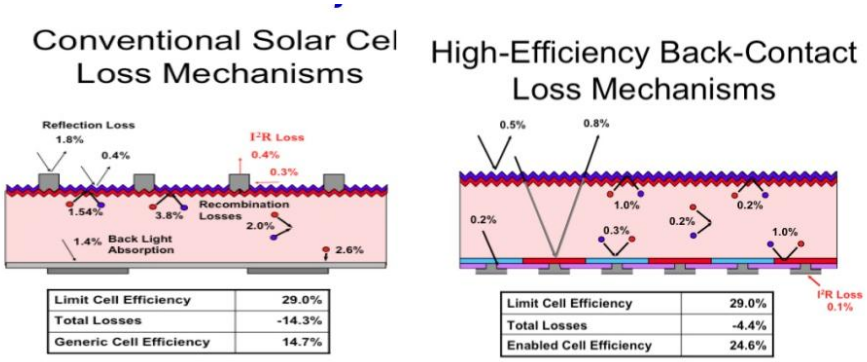

Fig. 1: Standard Front Junction vs All Back Contact

Project Achievements

Silicon Heterojunction Cell has been fabricated with an initial efficiency 13.24% on n-type flat silicon wafer. The project goal is to fabricate SHJ-IBC solar cell with the following structure.

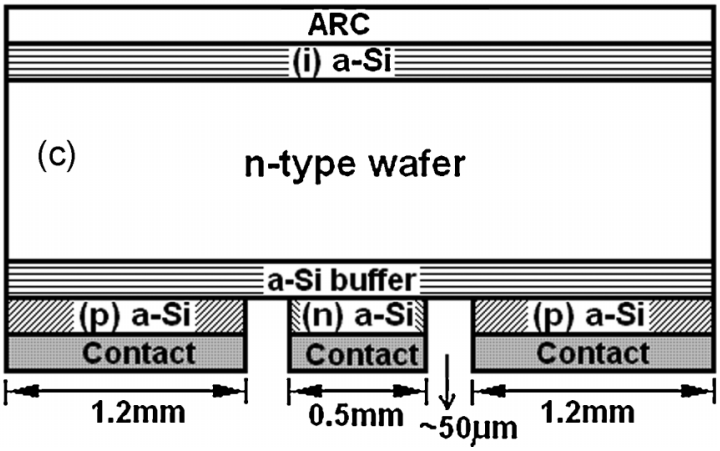

Fig. 2: Schematic Structure of Integrated Back Contact Solar Cells

Publications

1. “Silicon Heterojunction Solar Cells with novel Fluorinated n-type Nanocrystalline Silicon Oxide Emitters on p-type c-Si”, Sukanta Dhar, Sourav Mandal, Gourab Das, Chandan Banerjee, Sumita Mukhopadhyay A. K. Barua, Japanese Journal of Applied Physics 54, 08KD03 (2015).
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