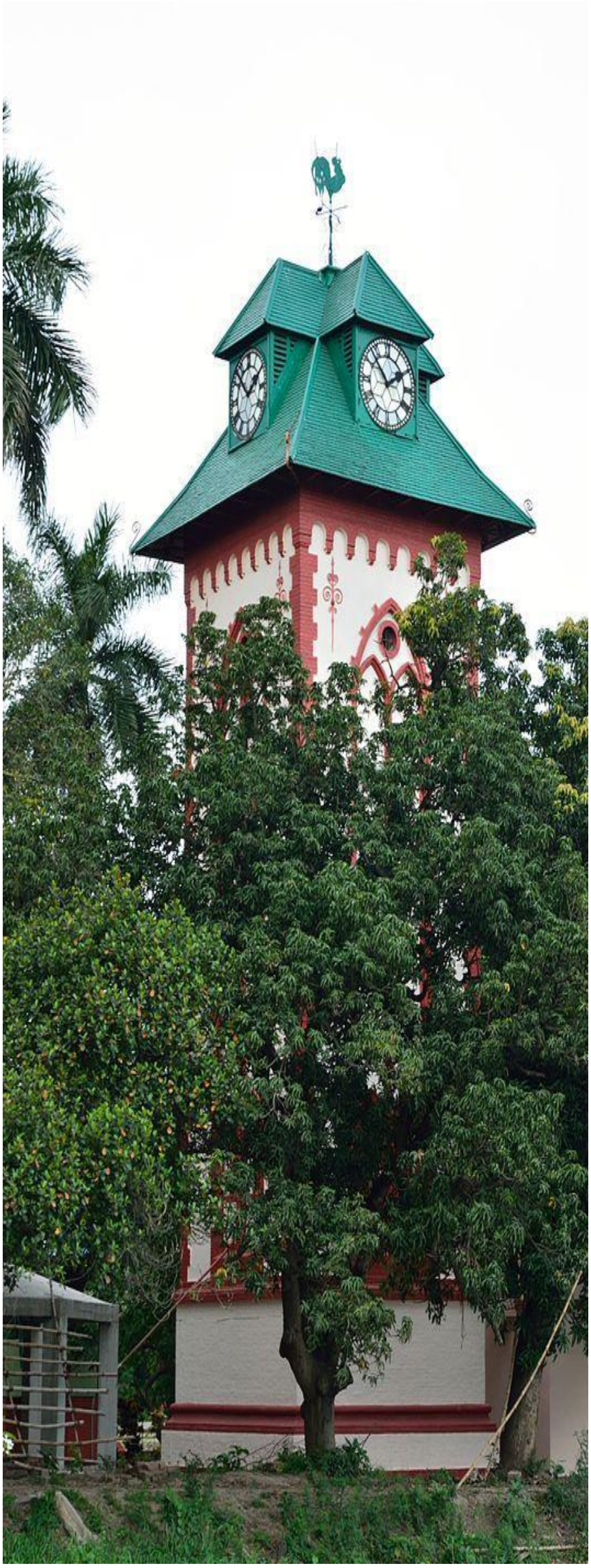

# School of VLSI Technology

## Postgraduate Programmes

**Course Structure and Syllabus**

(Effective from 2025-26 admitting batch onwards)

**Indian Institute of Engineering Science and Technology (IIEST), Shibpur**

**Botanic Garden, Howrah**

# Table of Contents

# Course Structure

## M.Tech in VLSI DESIGN

**COURSE STRUCTURE FOR M. TECH. IN VLSI DESIGN AT SCHOOL OF VLSI TECHNOLOGY**

***First Semester***

| Sl. No. | Type | Course Name | Course code | Class Load/Week L | T | P | Credit | Class load/ week | Marks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | PC | Semiconductor Devices and Modelling | VL5101N | 3 | 0 | 0 | 3 | 3 | 100 |
| 2 | PC | Analog VLSI Circuits | VL5102N | 3 | 0 | 0 | 3 | 3 | 100 |
| 3 | PC | Digital VLSI Circuits | VL5103N | 3 | 0 | 0 | 3 | 3 | 100 |
| 4 | PSE | * At least one will be offered | VL512XN | 3 | 0 | 0 | 3 | 3 | 100 |
| 5 | OE | ** At least one will be offered | VL516XN | 3 | 0 | 0 | 3 | 3 | 100 |
| | | **Theory Sub-total** | | **15** | **0** | **0** | **15** | **15** | **500** |
| 6 | PC | Lab-1 Semiconductor Devices and Modelling Lab | VL5171N | 0 | 0 | 3 | 2 | 3 | 50 |
| 7 | PC | Lab-2 Analog VLSI Circuits Lab | VL5172N | 0 | 0 | 3 | 2 | 3 | 50 |
| 8 | PC | Lab-3 Digital VLSI Circuits Lab | VL5173N | 0 | 0 | 3 | 2 | 3 | 50 |
| | | **Practical Sub-total** | | **0** | **0** | **9** | **6** | **9** | **150** |
| | | **First Semester Total** | | **15** | **0** | **9** | **21** | **24** | **650** |

***Second Semester***

| Sl. No. | Type | Course Name | Course code | Class Load/Week L | T | P | Credit | Class load/ week | Marks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | PC | VLSI Physical Design | VL5201N | 3 | 0 | 0 | 3 | 3 | 100 |
| 2 | PC | IC Technology | VL5202N | 3 | 0 | 0 | 3 | 3 | 100 |
| 3 | PC | Testing and Verification | VL5203N | 3 | 0 | 0 | 3 | 3 | 100 |
| 4 | PSE | * At least one will be offered | VL522XN | 3 | 0 | 0 | 3 | 3 | 100 |
| 5 | OE | ** At least one will be offered | VL526XN | 3 | 0 | 0 | 3 | 3 | 100 |
| | | **Theory Sub-total** | | **15** | **0** | **0** | **15** | **15** | **500** |
| 6 | P | M.Tech. project/Term-paper | VL5291N | 0 | 0 | 3 | 2 | 3 | 50 |
| 7 | O | Seminar/Viva Voce | VL5292N | 0 | 0 | 3 | 2 | 3 | 50 |
| | | **Practical Sub-total** | | **0** | **0** | **6** | **4** | **6** | **100** |
| | | **Second Semester Total** | | **15** | **0** | **6** | **19** | **21** | **600** |

***Third Semester***

| Sl. No. | Type | Course Name | Course code | Class Load/Week L | T | P | Credit | Class load/ week | Marks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **VAC** | | | 3 | 0 | 0 | 3 | 3 | 100 |
| 2 | P | M. Tech. Thesis | VL6191N | | | | 12 | 24 | 300 |
| 3 | O | Progress Seminar and Viva-voce | VL6192N | | | | 6 | | 100 |
| 4 | I | Summer internship (6-8 weeks) evaluation | VL6193N | | | | 2 | | 50 |
| | | **Third Semester Total** | | | | | **23** | | **550** |

***Fourth Semester***

| Sl. No. | Type | Course Name | Course code | Class Load/Week L | T | P | Credit | Class load/ week | Marks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | P | M. Tech. final thesis | VL6291N | | | | 22 | 30 | 400 |
| 2 | O | Thesis Seminar and Viva-voce | VL6292N | | | | 8 | | 200 |
| | | **Fourth Semester Total** | | | | | **30** | | **600** |

**Type of courses**

- Basic Science Course (BSC)
- Engineering Science Course (ESC)
- Humanities and Social Sciences Course (HSC)
- Program Core Courses (PC)
- Program Specific Elective Course (PSE)
- Open Electives (OE)
- Value Added Course (VAC)
- Project (P)
- Internship (I)
- Other (O) such as seminar, viva voce, etc.

| 1st SEMESTER | 2nd SEMESTER |
|---|---|
| **A. PSE** | **A. PSE** |
| 1. Advanced Systems Architecture | 1. Low Power Design |
| 2. Embedded Systems and IOT | 2. Mixed signal circuit design |
| 3. Nano and Molecular Electronics | 3. RF IC design |
| 4. Hardware Security | 4. SOC Design and Testing |
| 5. VLSI Interconnects | 5. Emerging Technologies |
| **B. OE** | **B. OE** |
| 1. MEMS and Microsystems | 1. VLSI Architecture for DSP |
| 2. Quantum Computing | 2. FPGA system design |
| 3. Logic Synthesis and Verification | |

# M.Tech in VLSI DESIGN

## Detailed Syllabus

# M.Tech in VLSI DESIGN (1st SEMESTER)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Course Code** | VL5101N | **Course Name** | Semiconductor Device and Modeling | **Course Category** | PC | L | T | P |
| | | | | | | 3 | 0 | 0 |

| | | | | | |
|---|---|---|---|---|---|
| **Pre-requisite Courses** | Basic Electronics, Solid State Physics | **Co-requisite Courses** | Semiconductor Devices and Modelling Lab | **Progressive Courses** | IC technology |
| **Course Offering Department** | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard Semiconductor Data Manuals, Manufacturer Datasheets |

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| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Crystals and Band structures: Crystal Structure, Lattice, Lattice with basis, Band structure evolution, E-k relation, Density of states, Carrier Statistics | 8 | Summarize the core theoretical principles introduced in this module. |
| 2 | Semiconductors in Equilibrium and Carrier Transport in Semiconductors: Semiconductor Materials, Carrier Concentration, Carrier Drift, Carrier Diffusion, Generation and Recombination Process, Continuity Equation, Thermionic Emission, Tunnelling, Ballistic Transport, High Field Effects | 8 | Analyze the system behavior using appropriate models and simulation techniques. |
| 3 | Physics of Junction Devices: Thermal Equilibrium Condition, Depletion Region, Depletion and Diffusion Capacitances, Current-Voltage Characteristics, Charge Storage and Transient Behaviour, Junction Breakdown, Metal Semiconductor Contacts | 8 | Design and optimize key circuit or system components introduced in the module. |
| 4 | Physics of Bipolar devices: Transistor Action, Static Characteristics, Frequency Response and Switching, Hetero junction | 4 | Evaluate performance metrics and trade-offs related to the given topic. |

| | | | |
|---|---|---|---|
| 5 | MOS Electrostatics in two terminal MOS structure: Energy band diagram in equilibrium and under bias, Flat band voltage, Potential Balance and charge balance, Effect of gate body voltage on surface condition, Accumulation and depletion, Inversion, CV Characteristics, Frequency response | 6 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 6 | Three terminal MOS Structure: Introduction, Contacting the Inversion layer, the body effect, Regions of inversion, V_CR control | 2 | Describe the foundational concepts and contextual relevance of the module topic. |
| 7 | Four terminal MOS Structure: Introduction, Transistor region of operation, Complete all region model, Simplified all region models, Model based on Quasi-Fermi Potential, Regions of inversion in term of terminal voltages, strong inversion, weak inversion, moderate inversion, source referenced vs body referenced modelling, effective mobility, temperature effects | 6 | Describe the foundational concepts and contextual relevance of the module topic. |
| 8 | Small Dimension Effects: Introduction, carrier velocity saturation, channel length modulation, charge sharing, drain induced barrier lowering punch through, hot carrier effects, poly-silicon depletion, quantum mechanical effects, DC gate current, junction leakage: band to band tunnelling and GIDL, leakage currents | 4 | Describe the foundational concepts and contextual relevance of the module topic. |
| 9 | Ballistic FET: Introduction, channel transmission, Introduction to the Virtual source model | 2 | |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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|---|---|
| **Learning Resources** | Text Books:<br>- Introduction to Semiconductor Materials and devices by M.S Tyagi, John Wiley & Sons, 5th Edition, 2005.<br>- Semiconductor Devices: Modeling and Technology by A Dasgupta, N. Dasgupta, Prentice Hall India Private Limited, 2004.<br>- Solid State Physics By Neil W. Ashcroft, N. David Mermin, Cengage Learning, 2011.<br>- Operation and modeling of the MOS transistor by Yannis Tsividis, Oxford University Press, 2011.<br><br>Reference Books:<br>- Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, John Wiley & Sons, 3rd Edition, 2002.<br>- Solid State Electronic Devices by Ben G. Streetman and Sanjay Banerjee, |

| | |
|---|---|
| | Prentice Hall, 6th Edition 2005.<br>- Semiconductor Device Fundamentals by Robert F. Pierret, Addison-Wesley Publishing, 1996.<br>- Semiconductor Physics and Devices by Donald A. Neamen, McGrawHill, 3rd Edition 2003.<br>- Semiconductor Devices- Basic Principles by Jasprit Singh, John Wiley and Sons Inc., 2001.<br>- Semiconductor Devices- Physics and Technology, by S. M. Sze and M.K. Lee, John Wiley & Sons, 3rd Edition, 2012.<br>- Fundamental of Modern VLSI devices by Yuan Taur and Tak H. Ning, Cambridge University Press, 2nd Edition, 1998. |

| **Course Code** | VL5102N | **Course Name** | Analog VLSI Circuits | **Course Category** | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| **Pre-requisite Courses** | Circuit Theory, Basic Electronics | **Co-requisite Courses** | Analog VLSI Circuits Lab | **Progressive Courses** | Mix-Signal Design |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Cadence Design Manual, Analog IC Design References |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| **Module** | **Syllabus** | **Duration (class-hour)** | **Module Outcome** |
|---|---|---|---|
| 1 | Introduction: Basic MOSFET device, characteristics, second order effects, MOS device model | 4 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Amplifiers: Low frequency and high frequency operation of single stage amplifier and differential amplifier (i) Single stage amplifiers: common source (CS), source follower, common gate stage, | 6 | Apply advanced concepts to solve |

| | | | |
|---|---|---|---|
| | cascade stage with different load; (ii) Differential Amplifiers: Basic differential operation, common mode response, Current mirror, differential amplifier with current mirror load | | domain-specific VLSI problems. |
| 3 | Noise analysis: Statistical characteristic of noise, thermal noise, Flicker noise, representation noise in circuits | 3 | Assess noise sources and develop mitigation strategies for signal integrity. |
| 4 | Operational amplifier: one stage OPAMP, two stage OPAMP, gain boosting, common mode feedback, slew rate, power supply rejection | 3 | Apply techniques to reduce dynamic and static power in VLSI systems. |
| 5 | Bandgap references: Supply independent biasing, temperature independent references, PTAT and CTAT current generation | 4 | Design and optimize key circuit or system components introduced in the module. |
| 6 | Switched capacitor circuits: Sampling switches, switched capacitor amplifier, switched capacitor integrator | 3 | Evaluate performance metrics and trade-offs related to the given topic. |
| 7 | Oscillators: Feedback and Stability, Ring Oscillator, L-C oscillator, Voltage Control oscillator, phase locked loop, Building blocks, locking characteristics and design | 5 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 8 | Comparator: Simple, Switch-based and latch based | 3 | Summarize the core theoretical principles introduced in this module. |
| 9 | Data Converter: Characterization of ADC and DAC, ADC and DAC architectures | 3 | Implement architectural strategies and assess their performance. |
| 10 | Power Management: LDO and DC-DC Converters | 3 | Assess techniques to reduce and optimize power consumption. |

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|---|---|---|---|
| 11 | Active Filters: Design of switch capacitor filter, Design of OTA-C filter | 3 | Design and evaluate systems or components introduced in this module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw Hill, 2003.<br>- CMOS Analog Circuit Design by P.E Allen and Douglas R. Holdberg, Oxford University Press, 2nd edition, 2012.<br><br>Reference Books:<br>- Analysis and Design of Analog Integrated Circuits by Paul Gray and Robert G Meyer, John Wiley & Sons, 2009.<br>- Analog Circuit Design by Johan Huijsing Rudy van Plassche and Willy Sansen, Springer Science and Business Media, B.V. |

| Course Code | VL5103N | Course Name | Digital VLSI Circuits | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital Electronics, Computer Architecture | Co-requisite Courses | Digital VLSI Circuits Lab | Progressive Courses | Testing and Verification, VLSI Physical Design |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | CMOS Design Manuals, Verilog HDL Reference |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Combinational logic design: Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates- dynamic or glitching transitions - Design techniques to reduce switching activity - Ratioed logic-pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor- Dynamic CMOS design-Basic principles -Domino logic-optimization of Domino logic-NPCMOS-logic style – Voltage scaling. | 10 | Apply techniques to reduce dynamic and static power in VLSI systems. |
| 2 | Sequential logic design: Timing metrics for sequential circuit -latches Vs registers -static latches and registers – Bi-stability principle - multiplexer based latches-master slave | 10 | Analyze timing constraints and apply synthesis optimizations for robust digital design. |

| | | | |
|---|---|---|---|
| | edge triggered registers- nonideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-CMOS register -Dual edge registers-True single phase clocked registers. | | |
| 3 | Semiconductor Memories: Dynamic Random Access Memories RAM, non-volatile memories, flash memories, lowpower memory | 8 | Examine memory architectures and assess design techniques for SRAM/DRAM systems. |
| 4 | CMOS subsystem design: Data Path Operations: Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Pipeline multiplier array, Booth"s algorithm, Finite-State Machines. | 6 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 5 | HARDWARE MODELING WITH THE VERILOG HDL : Hardware –The Verilog Module, Descriptive Styles, Structural Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Verilog for RTL Synthesis. | 6 | Implement hardware descriptions using Verilog HDL and test functional correctness. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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|---|---|
| **Learning Resources** | Text Books:<br>- CMOS VLSI Design - A Circuits and Systems Perspective by Neil H Weste, D Harris and Ayan Banerjee, Pearson, 2012.<br>- Digital Integrated Circuits- A Design Perspective by J M Rabaey, Prentice Hall, 3rd Edition, 2012.<br>- FPGA based systems, Waney Wolf, Pearson, 1st ed, 2005.<br>- Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital IC-Analysis and Design", Tata McGraw Hill publication.<br><br>Reference Books:<br>- M.D. CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PrenticeHall.<br>- M.G. ARNOLD, "Verilog Digital - Computer Design", Prentice-Hall. |

| Course Code | VL-5121N | Course Name | Advanced Systems Architecture | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Computer organisatio n | Co-requisite Courses | Compute r Architect ure | Progressive Courses | Advanced SoC Architecture |
|---|---|---|---|---|---|
| Course Offering Department | | School of VLSI Technology | | Data Book / Codes/Standards | H. Patterson |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| **1.** | **Overview of von Neumann architecture:** CISC and RISC processors, Instruction set architecture; Architecture, Measuring and reporting performance, Data Path Design. | **8** | Describe the foundational concepts and contextual relevance of the module topic. |
| **2.** | **Pipelining:** Basic concepts of pipelining, data hazards, control hazards, and structural hazards; Techniques for overcoming or reducing the effects of various hazards. | **6** | Design and optimize key circuit or system components introduced in the module. |
| **3.** | **Hierarchical Memory Technology:** Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies. | **8** | Examine memory architectures and assess design techniques for SRAM/DRAM systems. |
| **4.** | **Instruction-level parallelism:** Concepts of instruction-level parallelism (ILP), Techniques for increasing ILP; Superscalar, superpipelined and VLIW processor architectures; Vector and symbolic processors; Case studies of contemporary microprocessors. | **8** | Apply advanced concepts to solve domain-specific VLSI problems. |
| **5.** | **Multiprocessor Architecture:** Taxonomy of parallel architectures; Centralized shared-memory | **6** | Examine memory |

| | | | |
|---|---|---|---|
| | architecture, synchronization, memory consistency, interconnection networks; Distributed shared-memory architecture, Cluster computers. Multi-core architectures. | | architectures and assess design techniques for SRAM/DRAM systems. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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|---|---|
| **Learning Resources** | TEXT BOOKS<br>1. Computer Architecture: A quantitative approach – John L. Hennessy, David A. Patterson<br>– Morgan Kaufmann<br>2. Computer organization and Architecture : Designing for performance William Stallings<br>– Pearson<br>3. Advanced Computer Architecture : Parallelism, Scalability and programmability Kai<br>REFERENCE BOOKS<br>1. Computer Organization and design : The Hardware/Software Interface, David A.<br>Patterson, John L. Hennessy -Morgan Kaufmann, Year: 2004 |

| Course Code | VL5122N | Course Name | Embedded Systems and IoT | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Microprocessor and Microcontroller | Co-requisite Courses | Digital VLSI Circuits | Progressive Courses | SoC Design |
|---|---|---|---|---|---|
| Course Offering Department | | *School of VLSI Technology* | | Data Book / Codes/Standards | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction: Features, Design metrics, Design flow | 2 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Microcontroller Systems: ARM Instruction set architecture, ARM pipeline, THUMB instructions, Exceptions in ARM, Raspberry Pi, Arduino based system design (drone based applications) | 5 | Design and optimize key circuit or system components introduced in the module. |
| 3 | Digital Signal Processors: Architecture, Data access features, Computation features, Accuracy, C6000 family of DSP | 4 | Evaluate performance metrics and trade-offs related to the given topic. |
| 4 | Field Programmable Gate Arrays: Field programmable devices, Programmability, Logic block variations, Design flow, Modern FPGAs, Concept of soft and hard IP | 5 | Apply advanced concepts to solve |

| | | | |
|---|---|---|---|
| | | | domain-specific VLSI problems. |
| 5 | Interfacing: Requirements, SPI, IIC, RS232-C family, USB, IrDA, CAN, Bluetooth, PCI | 7 | Summarize the core theoretical principles introduced in this module. |
| 6 | Real-time System Design: Task classification, Periodicity, Task scheduling, scheduling algorithms, Resource sharing, Commercial RTOS | 6 | Analyze the system behavior using appropriate models and simulation techniques. |
| 7 | Hardware-Software Codesign: Introduction to specification, partitioning and co-simulation | 3 | Describe the foundational concepts and contextual relevance of the module topic. |
| 8 | IoT Systems: Overview of IoT systems, wireless sensor network applications, IoT in Healthcare, automotive and IIoT, Smart Grid | 8 | Describe the foundational concepts and contextual relevance of the module topic. |

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|---|---|
| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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|---|---|
| **Learning Resources** | Text Books:<br>- Embedded System Design, by S. Chattopadhyay, 2nd Edition, 2014.<br>- Embedded System Design: A Unified Hardware/Software Introduction, Frank Vahid, Tony D Givargis Wiley, 2002.<br><br>Reference Books:<br>- Embedded System Design, P. Marwedel, 2003.<br>- Arnold Berger, "Embedded system design" - CMP books. |

| Course Code | VL5123N | Course Name | Nano and Molecular Electronics | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Basic Electronics and Device Physics | Co-requisite Courses | Semiconductor Devices. | Progressive Courses | IC Technology |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction: Nanotechnology and Nanoelectronics; Moore's Law; Review of Semiconductor Electronics; Maxwell's Equation, Poisson Equation, Continuity Equations, carrier concentration, Carrier Transport, Drift and diffusion; basics of molecular electronics | 4 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Basics of Quantum Mechanics: Photoelectric effect; Wave nature of particles and wave-particle duality; Compton Effect; Uncertainty Principle; Schrodinger's equations and its applications; Wave function and postulates; Pauli-exclusion principle; Quantum dots, wires, and wells; Transport in quantum structures; Optoelectronic property | 14 | Summarize the core theoretical principles introduced in this module. |
| 3 | Nanoelectronic Devices: Overview of MOS and MOSFET; CMOS Scaling and shrink down approaches; FINFET; Tunnel FET; Junctionless Transistor; Single electron transistors; Nanowire MOSFET, GAA FET | 10 | Describe the foundational concepts and contextual relevance of the module topic. |
| 4 | Molecular Electronics: Need of molecular electronics and atoms-up approach; Strategies of electronic development; Molecular bonding and hybridization; Molecules as electronic devices; Carbon molecules & electronics; Pentacene; Transport in molecular electronics; Graphene devices; Carbon nanotube electronics; CNT FET | 12 | Design and optimize key circuit or system components introduced in the module. |

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|---|---|
| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

| | |
|---|---|
| **Learning Resources** | Text Books:<br>- C.P. Poole Jr. and F.J. Owens, Introduction to Nanotechnology, Wiley, 2003.<br>- D.A. Neamen, Semiconductor Physics & Devices, TMH, 2003.<br>- Ashcroft and Mermin, Solid State Physics, Thomson Press (India) Ltd, 2003.<br>- G.W. Hanson, Fundamentals of Nanoelectronics, Pearson, 2009.<br>- M.C. Petty, Molecular Electronics: From Principles to Practice, Wiley, 2007.<br><br>Reference Books:<br>- C. Kittel, Introduction to solid state physics, Wiley, New York, 1976.<br>- K. Iniewski, Nanoelectronics: nanowires, molecular electronics, and nanodevices, McGraw Hill, New York, 2011.<br>- K. Sienicki, Molecular Electronics and Molecular Electronic Devices, CRC Press, 1994.<br>- S.M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981.<br>- J.H. Davies, The Physics of Low-Dimensional Semiconductors, Cambridge University Press, 1998.<br>- R.F. Pierrett, Semiconductor Device Fundamentals, Pearson, 2006.<br>- B.G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson, 2008. |

| Course Code | VL5124N | Course Name | Hardware Security | Course Category | Departmental Elective | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Cryptography, Digital Electronics | Co-requisite Courses | Digital VLSI Circuits | Progressive Courses | Testing and Verification |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Overview of Different Issues of Hardware Security | 2 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Preliminaries: Algebra of Finite Fields, Basics of the Mathematical Theory of Public Key Cryptography, Basics of Digital Design on Field-programmable Gate Array (FPGA), Classification using Support Vector Machines (SVMs) | 5 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 3 | Useful Hardware Security Primitives: Cryptographic Hardware and their Implementation, Optimization of Cryptographic Hardware on FPGA, Physically Unclonable Functions (PUFs), PUF Implementations, PUF Quality Evaluation, Design Techniques to Increase PUF Response Quality | 6 | Summarize the core theoretical principles introduced in this module. |
| 4 | Side-channel Attacks on Cryptographic Hardware: Basic Idea, Current-measurement based Side-channel Attacks [Case Study: Kochers Attack on DES], Design Techniques to Prevent Side-channel Attacks, Improved | 6 | Analyze the system behavior using |

| | | | |
|---|---|---|---|
| | Side-channel Attack Algorithms (Template Attack, etc.), Cache Attacks | | appropriate models and simulation techniques. |
| 5 | Testability and Verification of Cryptographic Hardware: Fault-tolerance of Cryptographic Hardware, Fault Attacks, Verification of Finite-field Arithmetic Circuits | 5 | Identify test strategies and fault models to ensure circuit reliability and coverage. |
| 6 | Modern IC Design and Manufacturing Practices and Their Implications: Hardware Intellectual Property (IP) Piracy and IC Piracy, Design Techniques to Prevent IP and IC Piracy, Using PUFs to prevent Hardware Piracy, Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs, Genetic Programming based Modeling of Ring Oscillator PUF) | 8 | Evaluate performance metrics and trade-offs related to the given topic. |
| 7 | Hardware Trojans: Hardware Trojan Nomenclature and Operating Modes, Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans, Logic Testing and Side-channel Analysis based Techniques for Trojan Detection, Techniques to Increase Testing Sensitivity Infrastructure Security: Impact of Hardware Security Compromise on Public Infrastructure, Defence Techniques (Case Study: Smart-Grid Security) | 8 | Identify test strategies and fault models to ensure circuit reliability and coverage. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, “Hardware Security: Design, Threats, and Safeguards”, CRC Press.<br><br>Reference Books:<br>- Ahmad-Reza Sadeghi and David Naccache (eds.): Towards Hardware-intrinsic Security: Theory and Practice, Springer.<br>- Ted Huffmire et al: Handbook of FPGA Design Security, Springer.<br>- Stefan Mangard, Elisabeth Oswald, Thomas Popp: Power analysis attacks - revealing the secrets of smart cards. Springer 2007.<br>- Doug Stinson, Cryptography Theory and Practice, CRC Press. |

| Course Code | VL5125N | Course Name | VLSI Interconnects | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Basic Electronics | Co-requisite Courses | Semiconductor Devices and Modelling | Progressive Courses | VLSI Physical Design |
|---|---|---|---|---|---|
| Course Offering Department | | *School of VLSI Technology* | | Data Book / Codes/Standards | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction to VLSI interconnects classification, Cu Interconnect, Technological trends, Interconnect scaling, Typical interconnect structure, Electromigration phenomenon, Signal transmission on interconnects, On-chip Interconnects, Package level interconnections | 5 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Extraction of interconnect parameters, Physics of interconnects in VLSI, physical foundations for circuit models of VLSI interconnects, Interconnect resistance, capacitance, inductance modelling, Extended Miller effect, Alternatives for extraction. Modelling interconnect drivers. Loss and Lossless transmission line model, Switch-level RC model. T and π network interconnect model. Effective capacitance modelling. Modelling interconnect wires. General interconnect network. An RC tree. The transfer function. Convolution of input and impulse response. Moments of the transfer function. Impulse and step response of RC tree. Elmore delay. Response of single RC. Elmore delay of 2-stage RC. RC-tree. Step response of lumped vs. distributed RC line. Sample RLC network. Modified node analysis equations | 15 | Design and evaluate clocking schemes and interconnects for performance and reliability. |
| 3 | Active and Passive interconnections, Multilevel and multilayer interconnections, Propagation delays, Crosstalk effects in digital circuits, spurious signals, | 8 | Design and evaluate clocking schemes and |

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| | crosstalk induced delay, energy dissipation due to crosstalk, crosstalk effects in logic VLSI circuits | | interconnects for performance and reliability. |
| 4 | Techniques for avoiding interconnection noise, noise detection problem, brief introduction to the testing of logic circuits, Crosstalk configuration, DC noise margins, Crosstalk-induced spurious signal detection, Reasons for high delay uncertainty, switch factor modelling of delay uncertainty, Buffer insertion for noise; Routing topology generation for speed optimization, Width optimization based on separability /monotonicity properties. Introduction to emerging interconnects (CNT, Graphene, optical interconnects and so on) | 12 | Describe the foundational concepts and contextual relevance of the module topic. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Grabinski, Hartmut, “Interconnects in VLSI Design”, 1st Edition, Springer, 2000.<br>- C-K. Cheng, J. Lillis, S. Lin, N. H. Chang, Interconnect Analysis and Synthesis J. Wiley, 2000.<br>- M. Celik, L. Pillegi, A. Odabasioglu. IC Interconnect Analysis. Kluwer, 2002.<br><br>Reference Books:<br>- A. B. Kahng, G. Robins. On Optimal Interconnections for VLSI. Kluwer, 1995.<br>- Moll, Francesc, Roca, Miquel, “Interconnection Noise in VLSI Circuits”, 1st Edition, Springer, 2004.<br>- J. A. Davis, J. D. Meindl. Interconnect Technology and Design for Gigascale Integration. Kluwer, 2003. F. Moll, M. Roca. Interconnection Noise in VLSI Circuits. Kluwer, 2004. |

| Course Code | VL-5161N | Course Name | MEMS and Microsystems | Course Category | OE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Analog Electronics, Solid-state Physics, Basic Electronics | Co-requisite Courses | Semiconductor Devices and Modeling | Progressive Courses | IC technology |
|---|---|---|---|---|---|
| Course Offering Department | | School of VLSI Technology | | Data Book / Codes/Standards | |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Scaling Laws, Why MEMS? | 2 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 2 | Microfabrication Techniques: Bulk micro machining, surface micro machining and LIGA processes | 6 | Summarize the core theoretical principles introduced in this module. |
| 3 | MEMS based inertial sensors: Accelerometer; piezoresistive and capacitive | 6 | Analyze the system behavior using appropriate models and simulation techniques. |
| 4 | MEMS based gyro and tilt sensors | 2 | Design and optimize key circuit or system components introduced in the module. |

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| 5 | MEMS based pressure sensor: (Type Pressure Monitoring System) | 2 | Evaluate performance metrics and trade-offs related to the given topic. |
| 6 | Electrostatic actuation: study of electrostatically actuated micro-machined cantilever beam: Free natural mode of vibration, resonance analysis, static voltage response, pull in and pull out phenomenon. Dynamic response to time varying electrostatic actuation | 4 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 7 | RF MEMS: RF switch, MEMS based inductor and capacitors, MEMS based varactors and resonators | 6 | Summarize the core theoretical principles introduced in this module. |
| 8 | Optical MEMS: MEMS based mirrors, MEMS based optical switch | 2 | Analyze the system behavior using appropriate models and simulation techniques. |
| **9.** | **Microfluidic and Bio MEMS:** advantages of MEMS based fluidic system. | **1** | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| **10.** | Micro pump and Micro valve, Micro nozzle and thrusters, micro needle, micro cantilever based bio sensors, lab on a chip | **5** | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| **11.** | **MEMS based interfacing electronics:** variable gain instrumentation amplifier and wireless integrated micro sensors | **4** | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | VLS161: MEMS and Microsystems)<br>- Total Duration: 40 class-hours<br>- Text Books:<br>- Analysis and design principles of MEMS devices by M.-H. Bao.<br>- Microsystem Design by Stephen D. Senturia, Kluwer Academic Publishers, 2001.<br>- Micro and Smart system by G. K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, Wiley, 2012.<br>- Fundamentals of Microfabrication techniques, Marc Madou, CRC Press. |

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| **Course Code** | VL5162N | **Course Name** | Quantum Computing | **Course Category** | OE | 3 | 0 | 0 |

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| **Pre-requisite Courses** | Quantum Physics | **Co-requisite Courses** | Nano and Molecular Electronics | **Progressive Courses** | Emerging Technologies |
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

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| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction to Quantum Computation: Foundations of quantum theory. States, observables, measurement and unitary evolution. Quantum bits, Bloch sphere presentation of a qubit, | 8 | Describe the foundational concepts and contextual |

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| | multiple qubits, Qubits versus classical bits, spin-half systems and photon polarisations. Pure and mixed states, density matrices | | relevance of the module topic. |
| 2 | Background Mathematics and Physics: Hilbert space, Probabilities and measurements, entanglement, density operators and correlation, basics of quantum mechanics, Measurements in bases other than computational basis, Extension to positive operator valued measures and super-operators. Decoherence and master equations. Quantum entanglement and Bell's theorems. Introduction to classical information theory and generalisation to quantum information | 8 | Describe the foundational concepts and contextual relevance of the module topic. |
| 3 | Quantum Circuits: single qubit gates, multiple qubit gates, design of quantum circuit, Reversible computation. Universal quantum logic gates and circuits, reversible to quantum circuit mapping, Quantum Gate library, Quantum circuit design constraints, Bennett embedding, Nearest Neighbour property, Launder Embedding Constraints | 8 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 4 | Quantum Algorithms: Classical computation on quantum computers. Relationship between quantum and classical complexity classes. Deutsch's algorithm, Deutsch's-Jozsa algorithm, Shor factorization, Grover search, Database search, FFT and prime factorization | 8 | Summarize the core theoretical principles introduced in this module. |
| 5 | Noise and error correction: Graph states and codes, Quantum error correction, Clifford +T group, fault-tolerant computation. Physical implementations of quantum computers | 8 | Assess noise sources and develop mitigation strategies for signal integrity. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Nielsen M. A., Quantum Computation and Quantum Information, Cambridge University Press.<br>- Pittenger A. O., An Introduction to Quantum Computing Algorithms 2000.<br>- Robert Wille, Rolf Drechsler- Towards a Design Flow for Reversible Logic - 2010 (Springer).<br><br>Reference Books:<br>- Benenti G., Casati G. and Strini G., Principles of Quantum Computation and Information, Vol. I: Basic Concepts, Vol II: Basic Tools and Special Topics, World Scientific. |

| Course Code | VL5163N | Course Name | Logic Synthesis and Verification | Course Category | OE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital Electronics | Co-requisite Courses | Digital VLSI Circuits | Progressive Courses | Testing and Verification |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Overview of the VLSI design flow | 1 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Register-Transfer Level (RTL) Behavioural, Dataflow and Structural synthesis | 2 | Analyze timing constraints and apply synthesis optimizations for robust digital design. |
| 3 | Hardware modeling principles and hardware description using the VHDL language | 6 | Implement hardware descriptions using Verilog HDL and test functional correctness. |
| 4 | Hardware modeling principles and hardware description using the Verilog language | 6 | Implement hardware descriptions using Verilog |

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| | | | HDL and test functional correctness. |
| 5 | 2-Level Logic Synthesis (Exact & Heuristic Two-Level Logic Minimization): SOP & POS forms: Costs & Characteristics, Implicants, Cubes and Covers, Quine-McCluskey Method, Minimum Cover via Unate Covering, Branch-and-Bound Methods, The ESPRESSO Minimizer | 5 | Analyze timing constraints and apply synthesis optimizations for robust digital design. |
| 6 | Sequential logic synthesis and state minimization using Finite state Machine (FSM) encoding algorithm | 3 | Analyze timing constraints and apply synthesis optimizations for robust digital design. |
| 7 | Retiming of sequential circuit synthesis | 3 | Analyze timing constraints and apply synthesis optimizations for robust digital design. |
| 8 | Technology mapping | 3 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 9 | Multi-level Logic synthesis: SIS, ABC, BDD | 3 | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| 10 | High-level Synthesis (HLS): DAG scheduling, Register allocation and binding, Datapath and controller design | 3 | Design and evaluate systems or components introduced in this module. |
| 11 | Verification: Introduction to formal methods for verification, BDD, Introduction and construction, OBDD, Operations on OBDD, OBDD for sequential circuits | 5 | Explain the fundamental concepts and objectives of the module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.<br>- Rudiger Ebendt, Gorschwin Fey, Rolf Drechsler. Advanced BDD Optimization, 2005.<br><br>Reference Books:<br>- S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.<br>- Douglas L. Perry, VHDL: Programming By Example 4th Edition, TMH.<br>- D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.<br>- Mano, M. Morris, "Digital Design", 3rd Edition, Prentice Hall PTR, 2001.<br>- Thomas H. Cormen, Clifford Stein, Ronald L. Rivest, Charles E. Leiserson, "Introduction to Algorithms", 2nd Edition, McGraw-Hill Higher Education, 2001.<br>- Gary D. Hachtel and Fabio Somenzi, Logic Synthesis and Verification Algorithms. Springer. |

| Course Code | VL5171N | Course Name | Semiconductor Devices and Modelling Lab | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
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| Pre-requisite Courses | Semiconductor Devices and Modelling | Co-requisite Courses | CAD tools simulation. | Progressive Courses | IC Technology |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Synopsis TCAD, Silvaco User Guides |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Practical experiments using Synopsis TCAD and Silvaco TCAD for device simulation and modeling (as per syllabus) | 36 | Utilize simulation tools effectively to model and evaluate circuit/system behavior. |

| Course Outcome | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| Learning Resources | Text Books:<br>- Standard academic textbook relevant to the course domain.<br><br>Reference Books:<br>- Additional reading materials and reference guides. |
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| Course Code | VL5172N | Course Name | Analog VLSI Circuits Lab | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
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| Pre-requisite Courses | Analog VLSI Circuits | Co-requisite Courses | CAD tools simulation. | Progressive Courses | Mix Signal VLSI Design |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Cadence Tool Manuals for Analog Circuit Design |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Practical experiments using Cadence Tools for analog circuit design (as per syllabus) | 36 | Utilize simulation tools effectively to model and evaluate circuit/system behavior. |

| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| **Learning Resources** | Text Books:<br>- Standard academic textbook relevant to the course domain.<br><br>Reference Books:<br>- Additional reading materials and reference guides. |
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| Course Code | VL5173N | Course Name | Digital VLSI Circuits Lab | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |

| Pre-requisite Courses | Digital VLSI Circuits | Co-requisite Courses | CAD tools simulatio n | Progressive Courses | VLSI Physical Design |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Cadence, Synopsis, Mentor Graphics Tool References |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Practical experiments using Cadence, Synopsis, and Mentor Graphics Design automation tools for digital circuit design (as per syllabus) | 36 | Utilize simulation tools effectively to model and evaluate circuit/system behavior. |

| Course Outcome | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| Learning Resources | Text Books:<br>- Standard academic textbook relevant to the course domain.<br><br>Reference Books:<br>- Additional reading materials and reference guides. |
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# M.Tech in VLSI DESIGN (2nd SEMESTER)

| Course Code | VL5201N | Course Name | VLSI Physical Design | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital Circuits and Systems | Co-requisite Courses | VLSI Interconnects | Progressive Courses | M.Tech Thesis Part II |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Physical Design Flow Documentation, Foundry PDK Manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction: VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Algorithmic complexity and optimization problems | 4 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Partitioning: Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing | 4 | Apply advanced concepts to solve domain-specific VLSI problems. |
| 3 | Floor planning: Problem formulation, Classification of floor planning algorithms, Constraint based floor planning, Rectangular dualization | 4 | Summarize the core theoretical principles introduced in this module. |
| 4 | Pin Assignment: Problem formulation, Classification of pin assignment algorithms, General and channel pin assignments | 4 | Analyze the system behavior using appropriate models and |

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| | | | simulation techniques. |
| 5 | Placement: Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms | 4 | Design and optimize key circuit or system components introduced in the module. |
| 6 | Global Routing and Detailed Routing: Global Routing: Problem formulation, Classification of global routing algorithms, Maze routing algorithms; Detailed Routing: Problem formulation, Classification of routing algorithms, Single layer routing algorithms | 4 | Evaluate performance metrics and trade-offs related to the given topic. |
| 7 | Physical Design Automation of FPGAs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing: Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Physical Design Automation of MCMs: Introduction to MCM Technologies, MCM Physical Design Cycle | 6 | Describe the foundational concepts and contextual relevance of the module topic. |
| 8 | Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention, packaging | 4 | Assess noise sources and develop mitigation strategies for signal integrity. |
| 9 | On Chip PDN Design: Noise and Decap Placement | 2 | Design and evaluate systems or components introduced in this module. |
| 10 | Lithography Aware Design: Design for Manufacturability | 4 | Design and evaluate systems or components introduced in this module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Algorithms for VLSI Physical Design Automation by Naveed Shervani, Springer International Edition, 3rd Edition, 2005.<br>- VLSI Physical Design Automation Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.<br>- FPGA based systems design, Waney Wolf, Pearson, 1st ed, 2005.<br><br>Reference Books:<br>- Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.<br>- VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.<br>- An Introduction to VLSI Physical Design - Majid Sarrafzadeh, C. K. Wong - Mc Graw Hill. |

| **Course Code** | VL5202N | **Course Name** | IC Technology | **Course Category** | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| **Pre-requisite Courses** | Semiconductor Devices and Modelling | **Co-requisite Courses** | VLSI Physical Design, Testing and Verification | **Progressive Courses** | Project Work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | VLSI Process Flow Manuals, Device Fabrication Standards |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| **Module** | **Syllabus** | **Duration (class-hour)** | **Module Outcome** |
|---|---|---|---|
| 1 | Introduction: Integrated Circuits and Planar Process, IC Families, CMOS Process Flow | 2 | Describe the foundational concepts and contextual relevance of the module topic. |
| 2 | Crystal Growth and Wafer Fabrication: Crystal Structure, Defects in Crystals, Raw materials and Purification, Czochralski and Float-Zone Crystal Growth Methods, Wafer Preparation and Specification, Measurement Methods | 6 | Design and optimize key circuit or system components introduced in the module. |
| 3 | Lithography: Light Sources, Wafer Exposure Systems, Photoresists, Mask Engineering, Measurement of Mask Features and Defects, Resist Patterns and Etched Features | 4 | Evaluate performance metrics and trade-offs related to the given topic. |
| 4 | Oxidation: Basic Concepts, Wet and Dry methods, Measurement Methods: Physical, Electrical and Optical, Models and Simulation: Linear and Parabolic, Growth Kinetics, Effect of Temperature, Pressure and Crystal Orientation | 2 | Utilize simulation tools effectively to model and |

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| | | | evaluate circuit/system behavior. |
| 5 | Diffusion: Dopant Solid Solubility, Fick's Law, Predeposition and drive-in, Gaussian Solution near a Surface, Measurement Methods: SIMS, Spreading Resistance, Sheet Resistance, and Capacitance Voltage | 4 | Summarize the core theoretical principles introduced in this module. |
| 6 | Ion Implantation: Role of Crystal Structure, High-Energy Implants, Ultralow Energy Implants, Ion Beam Heating, Measurement Methods, Models: Nuclear Stopping, Electronic Stopping, Damage and annealing | 2 | Analyze the system behavior using appropriate models and simulation techniques. |
| 7 | Deposition: Manufacturing Methods, CVD, APCVD, LPCVD, PECVD, PVD, Epitaxial Silicon, MBE, MOCVD, Polycrystalline Silicon, dielectrics and metals, Measurement and models | 6 | Design and optimize key circuit or system components introduced in the module. |
| 8 | Etching: Wet, Plasma Etching, Etching of Various Films, Measurement and Models | 4 | Evaluate performance metrics and trade-offs related to the given topic. |
| 9 | Back-end technology: Contacts, Interconnects and Vias, Silicide Gates and Source/Drain Regions, IMD Deposition and Planarization, Chemical-Mechanical Polishing, Electro-migration, Measurement methods | 6 | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| 10 | Wafer Processing, Process Variation and DFM | 3 | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Silicon VLSI Technology by James Plummer, M. Deal and P. Griffin, Prentice Hall Electronics and VLSI series, 2009.<br>- Semiconductor Devices: Basic Principles, Wiley Student edition, Paperback, 2007, Jasprit Singh.<br>- VLSI Technology, by S M Sze, McGraw-Hill, 1988.<br><br>Reference Books:<br>- The Science and Engineering of Microelectronics, by Stephen Campbell, Oxford University Press, 1996.<br>- VLSI Fabrication Principles by Sorab K Ghandhi, John Wiley and Sons, 2nd Edition, 1994.<br>- Microchip Fabrication by Peter van Zant, McGraw-Hill, 6th edition, 2013. |

| Course Code | VL5203N | Course Name | Testing and Verification | Course Category | PC | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 4 | 0 | 0 |

| Pre-requisite Courses | Digital Circuits and Systems | Co-requisite Courses | VLSI Physical Design | Progressive Courses | M.Tech Thesis Part II |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Test Bench Libraries, ATPG Tool User Manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction to VLSI Testing: Role of testing, Verification Vs Testing, Levels of testing, Overheads of testing, Basic testing principle, Ideal tests Vs Real Test | 5 | Explain the fundamental concepts and objectives of the module. |
| 2 | Fault Modeling: Defects, Errors and Faults, Functional Vs Structural Testing, Levels of Fault Models, Various types of faults, Fault Coverage, Fault Efficiency, Single Stuck-at Fault (Fault Equivalence, Equivalence of Single Stuck at Faults, Fault Collapsing, Fault Dominance, Fault dropping, Check point Theorem), Soft errors | 5 | Apply testing or verification strategies to ensure system reliability. |
| 3 | Logic and Fault Simulation: Role of simulation in design verification and test evaluation, True value/logic simulation, Algorithms for logic simulation, Fault simulation, Algorithms for fault simulation | 5 | Design and evaluate systems or components introduced in this module. |
| 4 | Testability Analysis: Controllability and Observability, Measures for controllability and observability of combinational circuits, Measures for controllability and observability of sequential circuits; Test Generation for Combinational Circuits; Definition of ATPG, ATPG algorithms for combinational circuits (Roth’s D algorithm), and Some applications | 5 | Analyze the characteristics and implications of the topic under study. |
| 5 | Test Generation for Sequential Circuits: Classical approach, DFT (Design for Testability) approach, Time Frame Expansion Method, Complexity of ATPG, and Example of Cyclic Circuit | 5 | Design and evaluate systems or components introduced in this module. |

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| 6 | Design for Testability: Design for Testability, Adhoc design, Generic scan based design, Classical scan based design, System level DFT approaches. Built In Self Test (BIST), BIST Techniques, BIST Response Compaction, Circular BIST, Overview of Memory BIST | 6 | Explain the fundamental concepts and objectives of the module. |
| 7 | Recent trends in Testing and Diagnosis: Machine learning approaches | 4 | Apply testing or verification strategies to ensure system reliability. |
| 8 | Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification, Mixed signal design verification (System Verilog, Verilog AMS) | 5 | Design and evaluate systems or components introduced in this module. |
| 9 | Basics of equivalence checking and model checking. Hardware emulation | 5 | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| **Course Outcome** | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| **Learning Resources** | Text Books:<br>- A Roadmap for formal property verification, Pallab Das Gupta, Springer, 1st ed, 2006 with NPTEL lectures.<br>- Essentials of electronic testing for digital, memory and mixed signal VLSI circuits, M L Bushnell and V D Agarwal, Springer, 1st ed, 2002.<br><br>Reference Books:<br>- Testing and Diagnosis of VLSI and ULSI, F. Lombardi, M.G. Sami, Springer, 1988. |

| Course Code | VL-5221N | Course Name | Low Power Design | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital VLSI Circuits, Analog VLSI Circuits | Co-requisite Courses | VLSI Physical Design | Progressive Courses | M.Tech Thesis |
|---|---|---|---|---|---|
| **Course Offering Department** | | **School of VLSI Technology** | | **Data Book / Codes/Standards** | |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| **1.** | **Introduction:** Low power and its applications; Algorithmic, Architectural, Gate and Physical Level power reduction approaches. | **6** | Explain the fundamental concepts and objectives of the module. |
| **2.** | **Sources of Power Dissipation:** Dynamic Power Dissipation: Short Circuit Power, Switching Power, Gliching Power; Static Power Dissipation, Degrees of Freedom. | **8** | Assess techniques to reduce and optimize power consumption. |
| **3.** | **Supply Voltage Scaling Approaches:** Device feature size scaling, MultiVdd Circuits, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management. | **8** | Assess techniques to reduce and optimize power consumption. |
| **4.** | **Switched Capacitance Minimization Approaches:** Hardware Software Tradeoffs, Bus Encoding Two's complements verses Sign Magnitude, Clock Gating. | **8** | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| **5.** | **Leakage Power minimization Approaches:** Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS). | **6** | Assess techniques to reduce and optimize power consumption. |
| **6.** | **Low Power Design Examples:** Memory, Arithmetic circuits. | **4** | Design and evaluate systems or components |

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| | | | introduced in this module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>1. Low Power VLSI CMOS Circuit Design, by A. Bellamour, and M. I. Elmasry, Springer Science<br>+ Business Media, 2012.<br>2. Low Power Design Essentials (Integrated Circuits and Systems), by Jan Rabaey, Springer,<br>2009.<br>Reference Books:<br>1. Principles of CMOS VLSI Design, by Neil H. E. Weste and K. Eshraghian, Addison Wesley<br>(Indian reprint).<br>2. CMOS Digital Integrated Circuits, by Sung Mo Kang, Yusuf Leblebici,Tata McGraw Hill.<br>3. Low Power Digital CMOS Design, by Anantha P. Chandrakasan and Robert W. Brodersen,<br>Kluwer Academic Publishers, 1995.<br>4. Low Power CMOS VLSI circuit design by Kaushik Roy, Sharat C. Prasad, John Willy & Sons,<br>2009. |

| Course Code | VL5222N | Course Name | Mixed Signal Circuit Design | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital VLSI Circuits, Analog VLSI Circuit | Co-requisite Courses | Low power Design | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction: Signals, Filters and Tools: Sinusoidal Signals, Comb Filters, Representing Signals, Sampling and Aliasing | 4 | Explain the fundamental concepts and objectives of the module. |
| 2 | Filters: Continuous-time filters, Discrete-time filters, Analog and discrete-time signal processing, Analog integrated continuous-time and discrete-time (switched-capacitor) filters | 6 | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| 3 | Digital Converters: Basics of Analog to digital converters (ADC), Basics of Digital to analog converters (DAC), DACs, Successive approximation ADCs, Dual slope ADCs, High-speed ADCs: flash ADC, pipeline ADC and related architectures, High-resolution ADCs: delta-sigma converters | 8 | Implement architectural strategies and assess their performance. |
| 4 | Phase locked loops: Phase Detector Voltage Controller Oscillator, Loop Filter: XOR DPLL, PFD DPLL, System Concerns: Clock Recovery From NRZ Data, Delay-Locked Loops | 6 | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| 5 | VLSI Layout: Chip Layout: Regularity, Standard Cell Examples, Power and Ground Considerations, Layout Steps by Dean Moriarty: Planning and Stick Diagrams, Device Placement, Polish, Standard cells Versus cuestom Layout | 8 | Assess techniques to reduce and optimize power consumption. |
| 6 | Interconnects: Basics, application, RC delay and its model | 6 | Apply theoretical and practical knowledge to solve domain-specific challenges. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- CMOS mixed-signal circuit design by R. Jacob Baker, Wiley India, IEEE press, 2008.<br><br>Reference Books:<br>- Design of analog CMOS integrated circuits by Behzad Razavi, McGraw-Hill, 2003.<br>- CMOS circuit design, layout and simulation by R. Jacob Baker, Revised second edition, IEEE press, 2008.<br>- CMOS Integrated ADCs and DACs by Rudy V. dePlassche, Springer (Indian edition), 2005.<br>- Electronic Filter Design Handbook by Arthur B. Williams, McGraw-Hill, 1981.<br>- Design of analog filters by R. Schauman, Prentice-Hall 1990. |

| Course Code | VL5223N | Course Name | RF IC Design | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital and analog electronics | Co-requisite Courses | Mixed-Signal Circuit Design | Progressive Courses | project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | *School of VLSI Technology* | | Data Book / Codes/Standards | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction RF and Wireless Technology: Complexity, design and applications. Choice of Technology | 2 | Explain the fundamental concepts and objectives of the module. |
| 2 | Basic concepts in RF Design: Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion | 4 | Design and evaluate systems or components introduced in this module. |
| 3 | Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation | 10 | Apply testing or verification strategies to ensure system reliability. |

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|---|---|---|---|
| 4 | Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations | 6 | Design and evaluate systems or components introduced in this module. |
| 5 | Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonator-less VCO design. Quadrature and single-sideband generators | 6 | Design and evaluate systems or components introduced in this module. |
| 6 | Radio Frequency Synthesizers: PLLS, design of integer-N RF frequency synthesizer and frequency dividers | 5 | Design and evaluate systems or components introduced in this module. |
| 7 | Design issues in integrated RF filters: Some discussion on available CAD tools for RF VLSI designs; Prerequisite: (Analog VLSI Design) | 4 | Design and evaluate systems or components introduced in this module. |
| 8 | RF power amplifier and linearization techniques: Classification of power amplifiers, design of class AB and class E amplifier, various techniques of linearization in cartesian mode | 3 | Design and evaluate systems or components introduced in this module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- RF Microelectronics by B Razavi, Prentice-Hall PTR, 1998.<br>- The Design of CMOS Radio-Frequency Integrated Circuits, by T H Lee, Press, 1998.<br>- Power Amplifier by Cripp.<br><br>Reference Books:<br>- CMOS Circuit Design, Layout and Simulation, by R J Baker, H W Li, and D.E. Boyce, Prentice-Hall, 1998.<br>- Mixed Analog and Digital VLSI Devices and Technology by Y P Tsividis, McGraw Hill, 1996. |

| **Course Code** | VLS224N | **Course Name** | SoC Design and Testing | **Course Category** | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| **Pre-requisite Courses** | Digital VLSI Circuits | **Co-requisite Courses** | FPGA System Design | **Progressive Courses** | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| **Module** | **Syllabus** | **Duration (class-hour)** | **Module Outcome** |
|---|---|---|---|
| 1 | Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing, System level interconnection, An approach for SoC Design, System Architecture and Complexity | 6 | Explain the fundamental concepts and objectives of the module. |
| 2 | Hardware/software co-design: partitioning, real-time scheduling, hardware acceleration | 4 | Design and evaluate systems or components introduced in this module. |
| 3 | Memory Design for SoC - Overview of SoC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split - I, and D - Caches, Multilevel Caches, Virtual to real translation, SoC Memory System, Models of Simple Processor - memory interaction | 6 | Explain the fundamental concepts and objectives of the module. |

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|---|---|---|---|
| 4 | Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SoC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SoC Customization | 6 | Implement architectural strategies and assess their performance. |
| 5 | Transaction-Level Modeling (TLM), Electronic System-Level [ESL] languages: SystemC | 5 | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| 6 | SoC and IP integration, verification and test | 6 | Apply testing or verification strategies to ensure system reliability. |
| 7 | Network on Chips: Introduction, Components, NOC Layers, Topologies, Routing | 4 | Explain the fundamental concepts and objectives of the module. |
| 8 | 3D IC: Synthesis, Power management and test issues | 3 | Assess techniques to reduce and optimize power consumption. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Design of System on a Chip: Devices and Components, Ricardo Reis, 1st Edition, 2004, Springer.<br>- System on Chip Verification - Methodologies and Techniques, Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.<br>- Computer System Design System-on-Chip, Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.<br><br>Reference Books:<br>- Multiprocessor Systems-on-Chips, A. Jerraya and W. Wolf, eds., Morgan Kaufmann, 2004.<br>- ARM System on Chip Architecture, Steve Furber, 2nd Edition, 2000, Addison Wesley Professional.<br>- Network on Chip: The next generation System on Chip integration, Santanu Kundu, Santanu Chattopadhyay, CRC Press, Year: 2014. |

| Course Code | VL5225N | Course Name | Emerging Technologies | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Nano and Molecular Electronics | Co-requisite Courses | IC Technology | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Microfluidic biochips: Introduction to Microfluidics, Lab on Chip devices, Flow based and digital microfluidic biochips, Biochip actuation techniques, Biochip application, Design Automation techniques for DMFBs, Chip level design for biochips, Paper based and MEDA based biochips | 8 | Explain the fundamental concepts and objectives of the module. |
| 2 | Optical circuits: Fundamentals of optical switching and its applications, MZI and its application as an optical switch, reversibility and reversible circuit using MZI, optical logic gates | 8 | Apply theoretical and practical knowledge to solve domain-specific challenges. |
| 3 | Memristors: Introduction to Memristor - An overview to the Memristor technology and non-Von Neumann architecture. Memristive-Devices- Types of Memristor - RRAM, PCM, STTMRAM. Utility of using RRAM for in-memory computations. Computational models for RRAM- Introduction to VTEAM model and, Stanford memristor-models. Logic design techniques using memristor- IMPLY, MAGIC, MRL, MTL. Logic synthesis methodologies inside Memristive-memory- Introduction to logic synthesis tools - ABC, SIMPLE | 7 | Explain the fundamental concepts and objectives of the module. |

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|---|---|---|---|
| | MAGIC. Future possibilities-A huge possibility for energy efficient and, performance efficient non-Von Neumann machines of future | | |
| 4 | CNT/GNR: Graphene Basics, Introduction to Carbon nanotube (CNT) and Graphene nanoribbon, Single-Wall (SW) and Multi-Wall (MW) CNT, CNT based FET and interconnect, Single layer (SL) and Multi layer (ML) GNR, GNR based FET and interconnect. Introduction to modelling techniques and performance analysis of CNT and GNR based device and interconnect for high speed power aware VLSI design | 10 | Explain the fundamental concepts and objectives of the module. |
| 5 | Reversible logic: fundamentals of reversible logic and gates, Reversible logic synthesis and design of reversible circuits | 7 | Design and evaluate systems or components introduced in this module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Digital Microfluidic Biochips: Design Automation and Optimization, Krishnendu Chakrabarty, Tao Xu - CRC Press, 2010.<br>- Digital Microfluidic Biochips: Synthesis, Testing and reconfigurable Techniques, Krishnendu Chakrabarty, Fei Su - CRC Press/Taylor and Francis, 2007.<br>- Carbon Nanotube and Graphene Nanoribbon Interconnects, Debaprasad Das, Hafizur Rahaman, 1/e CRC Press.<br>- Memristor networks, Andrew Adamtzky, Leon Chua, World Scientific Press.<br>- Towards a Design Flow for Reversible Logic - Robert Wille, Rolf Drechsler-2010 (Springer).<br><br>Reference Books:<br>- Memristors and Memristive systems - R. Stanley Williams (auth.), Ronald Tetzlaff (eds.) Publisher: Springer-Verlag New York, Year: 2014.<br>- VLS26X: Open Elective (e.g., VLS261: VLSI Architecture for DSP)<br>- Total Duration: 42 class-hours<br>- Text Books:<br>- VLSI digital signal processing systems by K K Parhi, John Wiley & Sons, 1999.<br>- Reference Books:<br>- DSP with FPGA by U. Meyer-Baese, Springer, 2004. |

| Course Code | VL-5261N | Course Name | VLSI Architecture for DSP | Course Category | PSE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | DSP | Co-requisite Courses | VLSI Architecture | Progressive Courses | Project |
|---|---|---|---|---|---|
| Course Offering Department | | School of VLSI Technology | | Data Book / Codes/Standards | UYE Meyer Baese |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| **1.** | **Introduction:** Introduction to DSP systems, DSP application demand and scaled CMOS technologies, representation of DSP algorithms, DFT and FFT. | **3** | Explain the fundamental concepts and objectives of the module. |
| **2.** | **Iteration bound:** Introduction, data flow graph representations, loop bound and iteration bound, algorithms for computing iteration bound. | **4** | Explain the fundamental concepts and objectives of the module. |
| **3.** | **Pipelining and parallel processing:** Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power. | **5** | Explain the fundamental concepts and objectives of the module. |
| **4.** | **Retiming:** Introduction, properties, solving systems of inequalities, retiming techniques. | **6** | Explain the fundamental concepts and objectives of the module. |
| **5.** | **Unfolding:** Introduction, algorithm for unfolding, properties, critical path, unfolding and retiming, applications. | **6** | Explain the fundamental concepts and objectives of the module. |
| **6.** | **Folding:** Introduction, folding transformation, register minimization techniques, register minimization in folded architectures. | **6** | Explain the fundamental concepts and |

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| | | | objectives of the module. |
| **7.** | **Systolic Architecture Design:** Introduction, systolic array design methodology, FIR systolic arrays, scheduling vector, matrix multiplication and 2D systolic array design. | **4** | Explain the fundamental concepts and objectives of the module. |
| **8.** | **Bit level arithmetic architectures:** Introduction, parallel multipliers, bit serial multipliers, bit serial filter design and implementation, canonic signed digit arithmetic, distributed arithmetic. | **4** | Explain the fundamental concepts and objectives of the module. |
| **9.** | **Redundant Arithmetic:** Introduction, Redundant number representation, carry free radix-2 additions and subtractions, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architecture, data format conversion. | **4** | Explain the fundamental concepts and objectives of the module. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | **Text Books**<br>1. VLSI digital signal processing systems by K K Parhi, John Wiley & Sons, 1999.<br>**Reference Books:**<br>1. DSP with FPGA by U. Meyer-Baese, Springer, 2004 |

| Course Code | VL5262N | Course Name | FPGA System Design | Course Category | OE | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 3 | 0 | 0 |

| Pre-requisite Courses | Digital Circuits and Systems | Co-requisite Courses | SoC Design and Testing | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| 1 | Introduction: Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software | 10 | Explain the fundamental concepts and objectives of the module. |
| 2 | The Structure of FPGA: FPGA general description. Different kinds of FPGA packages. FPGA architecture. Internal hard modules of FPGA [CLB, Block RAM, DCM), their meanings and usage. Different kinds of I/O modules, their usage and configuration | 10 | Implement architectural strategies and assess their performance. |
| 3 | FPGA Design Flow: Architecture design. Project design using Verilog Hardware Description Language (HDL). Defining testing methodology and testbench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation | 10 | Design and evaluate systems or components introduced in this module. |
| 4 | Testing Methodology: Functional and gate level testing. SDF file description and usage | 5 | Apply testing or verification strategies to ensure system reliability. |
| 5 | FPGA Configuration: Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA | 5 | Apply theoretical and practical knowledge to |

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| | | | solve domain-specific challenges. |

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| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |

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| **Learning Resources** | Text Books:<br>- Scott Hauck and Andre Dehon. Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation (Systems on Silicon Book 1).<br><br>Reference Books:<br>- D. Amos, Au. Lesea, R. Richter. "FPGA-Based Prototyping Methodology Manual", 2011.<br>- D. Vega. FPGA 133 Success Secrets - 133 Most Asked Questions on FPGA - What You Need to Know. Emereo Publishing, 2014.<br>- V. Sklyarov, I. Skliarova, A. Barkalov, L. Titarenko. Synthesis and Optimization of FPGA-Based Systems. Springer; 2014.<br>- P. Chu Pong, "FPGA Prototyping By Verilog Examples", Xilinx Spartan, 3rd version, 2008.<br>- High-performance ASIC Prototyping Systems (HAPS) Datasheets.<br>- Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010.<br>- PLD, FPGA Datasheets. |

| Course Code | VL5257N | Course Name | M.Tech Thesis Part-I | Course Category | Project (P) | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 4 | 0 | 0 |

| Pre-requisite Courses | Prior VLSI courses | Co-requisite Courses | CAD tool simulatio n | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | *School of VLSI Technology* | | Data Book / Codes/Standards | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| | | | |

| Course Outcome | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| Learning Resources | LABORATORY TOOLS. |
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| **Course Code** | VL5258N | **Course Name** | Term Paper Seminar & Viva - Voce | **Course Category** | O | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 2 | 0 | 0 |

| **Pre-requisite Courses** | Prior VLSI courses | **Co-requisite Courses** | CAD tool simulatio n | **Progressive Courses** | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| **Module** | **Syllabus** | **Duration (class-hour)** | **Module Outcome** |
|---|---|---|---|
| | | | |

| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| **Learning Resources** | LABORATORY TOOLS. |
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| **Course Code** | VL6151N | **Course Name** | M.Tech Thesis – Part-II | **Course Category** | P | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 12 | 0 | 0 |

| **Pre-requisite Courses** | Prior VLSI courses | **Co-requisite Courses** | CAD tool simulation | **Progressive Courses** | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
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| **Module** | **Syllabus** | **Duration (class-hour)** | **Module Outcome** |
|---|---|---|---|
| | | | |

| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| **Learning Resources** | LABORATORY TOOLS. |
|---|---|

| Course Code | VL6152N | Course Name | Progress Report Seminar & Viva-Voce | Course Category | O | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 0 | 0 |

| Pre-requisite Courses | Prior VLSI courses | Co-requisite Courses | CAD tools simulatio n | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| | | | |

| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
|---|---|

| **Learning Resources** | LABORATORY TOOLS. |
|---|---|

| Course Code | VL6251N | Course Name | M.Tech Final Thesis | Course Category | P | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 22 | 0 | 0 |

| Pre-requisite Courses | Prior VLSI courses | Co-requisite Courses | CAD tools simulatio n | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| Course Objective | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| | | | |

| Course Outcome | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| Learning Resources | LABORATORY TOOLS. |
|---|---|

| Course Code | VL6252N | Course Name | Thesis Seminar & Viva-Voce | Course Category | O | L | T | P |
|---|---|---|---|---|---|---|---|---|
| | | | | | | 8 | 0 | 0 |

| Pre-requisite Courses | Prior VLSI courses | Co-requisite Courses | CAD tools simulation | Progressive Courses | Advanced VLSI design, project or thesis work |
|---|---|---|---|---|---|
| Course Offering Department | | ***School of VLSI Technology*** | | **Data Book / Codes/Standards** | Standard academic textbooks, IEEE standards or tool manuals |

| **Course Objective** | This course is designed to provide students with in-depth knowledge and practical skills in the field, enabling them to analyze, design, and implement relevant systems using modern tools and methodologies. |
|---|---|

| Module | Syllabus | Duration (class-hour) | Module Outcome |
|---|---|---|---|
| | | | |

| **Course Outcome** | 1. Analyze key concepts and methodologies relevant to the course.<br>2. Apply theoretical principles to real-world problem solving.<br>3. Design and evaluate systems, processes, or components effectively.<br>4. Communicate technical information clearly and professionally. |
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| **Learning Resources** | LABORATORY TOOLS. |
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