Testing and Design-for-Testability for Digital Integrated Circuits

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Overview

Integrated circuits are manufactured by a long sequence of high-precision and hence defect-prone processing steps. Hence, every individual semiconductor product needs to undergo stringent electrical tests to weed out the defective parts and guarantee outgoing product quality to the customer. The field of 'Design-for-Test' (DfT) is focused on developing economically adequate tests for ICs. These tests need to assure sufficient quality at acceptable test application costs, corresponding to the target application area (e.g., wireless consumer products have less stringent quality requirements, but also different test cost budgets than medical or aerospace products). As no IC can be released into high-volume production without an adequate manufacturing test, acceptable test development time is also of key importance.

Structural testing, in which tests are generated based on well-accepted defect-abstracting fault models, have largely replaced the traditional functional tests, because they can be generated automatically in relatively short time, achieve objectively better defect coverage, and (in case of failing tests) allow diagnosis algorithms to pinpoint the type and location of the failure root cause. The latter enables automatic high-volume diagnosis to create process learning and yield improvement.

One of the main challenges in IC testing is the limited accessibility from the chip pins into the internal circuitry inside the IC. To improve controllability and observability, extra 'DfT hardware' is added to the functional circuitry; this typically amounts to 5-10% of the silicon area. Scan design is the most common form of DfT design, whereby a test mode is added in which functional registers are concatenated into one or more shift registers that are accessible from the external test equipment. More advanced forms of DfT hardware include (i) 'wrappers' that allows modular testing of increasingly complex chips, (ii) on-chip de-compression of test stimuli and compression of test responses, (iii) circuitry that tests parts of the IC itself without the need for external test equipment ('built-in self-test' or BIST), and (iv) on-chip features for the benefit of the chip user.

This course, presented by a world-renowned speaker in the field with broad scientific and industrial experience, covers the fundamentals of IC test and DfT. The speaker has presented their course material at many international conferences, in courses at Duke University, as well as to practicing engineers at in-house courses in major companies.

Modules	**Module 1: Test Fundamentals : July 25 - July 27, 2016** **Module 2: Memory Test and BIST : July 28 - July 29, 2016** **Module 3: System Test and Core-Based Design : August 1 - August 3, 2016** **Module 4: Testing of Module Biochips :August 4- August 5, 2016** **Number of participants for the course will be limited to thirty.**
You Should Attend If…	▪ You are an industry practitioner involved in design-for-test (DfT) and test of integrated circuits. ▪ You are a Doctoral/post-graduate/undergraduate student, or faculty in electrical/electronic engineering and computer science/engineering from academic institution.
Fees	The participation fees for taking the course is as follows: **Participants from abroad : US $300** **Industry/ Research Organizations: Rs.20000** **Academic Institutions: Rs. 5000** **Students at all levels: Rs. 500** The above fee include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hr free internet facility. The participants will be provided with accommodation on payment basis.

The Faculty

Prof. Krishnendu Chakrabarty is the William H. Younger Distinguished Professor of Engineering in the Department of Electrical and Computer Engineering at Duke University, USA. In addition, he serves as the Executive Director of Graduate Studies in Electrical and Computer Engineering. His research interests include testing and design-for-testability of integrated circuits; digital microfluidics, biochips, and cyber-physical systems; smart manufacturing and optimization of enterprise systems.

Prof. Hafizur Rahaman is a Professor of Indian Institute of Engineering Science and Technology (IIEST), Shibpur, India. His research interest include design and testing of Integrated Circuits and nano-biochips, emerging nanotechnologies including reversible computing.

Course Co-ordinator

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