School of VLSI Technology

Indian Institute of Engineering Science and Technology, Shibpur

Proposed Course Structure for Two-Year M. Tech (VLSI Design) Program

Course Structure

Semester 1

No	Paper	Sub. Code	Subject Name	Credit Hours	Total Marks	Type
1	Paper I	VL5101	Semiconductor Devices and Modeling	4	100	Dep. Core
2	Paper II	VL5102	Analog VLSI Circuits	3	100	Dep. Core
3	Paper III	VL5103	Digital VLSI Circuits	3	100	Dep. Core
4	Paper IV	VL5104/ X	* At least two will be offered	3	100	Dep. Elective
5	Paper V	VL5105	** One will be offered	3	100	OpenElective
6	Lab I	VL5151	Semiconductor Devices and Modelling Lab	2	100	Lab I /Dep. Core- Paper I
7	Lab II	VL5152	Analog VLSI Circuits Lab	2	100	Lab II /Dep. Core- Paper II
8	Lab III	VL5153	Digital VLSI Circuits Lab	2	100	Lab III /Dep. Core- Paper III
	Total			**22**		

A. Departmental Elective

1. Advanced Systems Architecture
2. Embedded Systems and IOT
3. Nano and Molecular Electronics
4. Hardware Security
5. VLSI Interconnects

B. Open Elective

1. MEMS and Microsystems
2. Quantum Computing
3. Logic Synthesis and Verification

Semester 2

No	Paper	Sub. Code	Subject Name	Credit Hours	Total Marks	Type
1	Paper VI	VL5201	VLSI Physical Design	3	100	Dep. Core
2	Paper VII	VL5202	IC Technology	3	100	Dep. Core
3	Paper VIII	VL5203	Testing and Verification	4	100	Dep. Core
4	Paper IX	VL5204/X	*at least two will be offered	3	100	Dep. Elective
5	Paper X	VL5205	**One will be offered	3	100	Open Elective
7	Project	VL5257	M.Tech Thesis –Part 1	4	200	Term Paper
8	Project	VL5258	Term Paper Seminar and Viva Voce	2	100	
	Total			**22**		

A. Departmental Elective

1. Low Power Design
2. Mixed signal circuit design
3. RF IC design
4. SOC Design and Testing
5. Emerging Technologies

B. Open Elective

1. VLSI Architecture for DSP
2. FPGA system design

Semester 3

No	Paper	Sub. Code	Subject Name	Credit Hours	Total Marks	Type
1	Thesis	VL6151	M.Tech Thesis Part II	12	300	Progress Report
2	Thesis	VL6152	Progress Report Seminar & Viva Voce	6	100	
	Total			**18**		

Semester 4

No	Paper	Sub. Code	Subject Name	Credit Hours	Total Marks	Type
1	Thesis	VL6251	M.Tech Final Thesis	22	400	Thesis
2	Thesis	VL6252	Thesis Seminar & Viva Voce	8	200	
	Total			**30**		

Total Credit: 22+22+18+30 = 92

Syllabus of First Semester

VL5101 Semiconductor Devices and Modelling

L-T-P: 3-1-0 **Credit: 4**

Sl. No.	Module name and topic	No. of classes
1.	**Crystals and Bandstructures :** Crystal Structure, Lattice, Lattice with basis, Bandstructure evolution, E-k relation, Density of states, Carrier Statistics	8
2.	**Semiconductors in Equilibrium and Carrier Transport in Semiconductors:** Semiconductor Materials, Carrier Concentration, Carrier Drift, Carrier Diffusion, Generation and Recombination Process, Continuity Equation, Thermionic Emission, Tunnelling, Ballistic Transport, High Field Effects.	8
3.	**Physics of Junction Devices:** Thermal Equilibrium Condition, Depletion Region, Depletion and Diffusion Capacitances, Current-Voltage Characteristics, Charge Storage and Transient Behavior, Junction Breakdown, Metal Semiconductor Contacts	8
4.	**Physics of Bipolar devices:** Transistor Action, Static Characteristics, Frequency Response and Switching, Heterojunction.	4
5.	**MOS Electrostatics in two terminal MOS structure:** Energy band diagram in equilibrium and under bias, Flat band voltage, Potential Balance and charge balance, Effect of gate body voltage on surface condition, Accumulation and depletion, Inversion, CV Characteristics, Frequency response.	6
6.	**Three terminal MOS Structure:** Introduction, Contacting the Inversion layer, the body effect, Regions of inversion, V_{CB} control.	2
7.	**Four terminal MOS Structure:** Introduction, Transistor region of operation, Complete all region model, Simplified all region models, Model based on Quasi-Fermi Potential, Regions of inversion in term of terminal voltages, strong inversion, weak inversion, moderate inversion, source referenced vs body referenced modelling, effective mobility, temperature effects.	6
8.	**Small Dimension Effects:** Introduction, carrier velocity saturation, channel length modulation, charge sharing, drain induced barrier lowering, punch through, hot carrier effects, polysilicon depletion, quantum mechanical effects, DC gate current, junction leakage: band to band tunnelling and GIDL, leakage currents.	4
9.	**Ballastic FET:** Introduction, channel transmission, Introduction to the Virtual source model.	2
Total number of classes		**48**

Text Books:

1. Introduction to Semiconductor Materials and devices by M.S Tyagi, John Wiley & Sons, 5th Edition, 2005.
2. Semiconductor Devices: Modeling and Technology by A Dasgupta, N. Dasgupta, Prentice hall India Private Limited, 2004.
3. Solid State Physics By Neil W. Ashcroft, N. David Mermin, Cengage Learning, 2011.

4. Operation and modeling of the MOS transistor by Yannis Tsividis, Oxford University Press, 2011

Reference Books:

1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, John Wiley & Sons, 3rd Edition, 2002.
2. Solid State Electronic Devices by Ben G. Streetman and Sanjay Banerjee, Prentice Hall, 6th Edition 2005.
3. Semiconductor Device Fundamentals by Robert F. Pierret, Addison-Wesley Publishing, 1996
4. Semiconductor Physics and Devices by Donald A. Neamen, McGrawHill, 3 rd Edition 2003
5. Semiconductor Devices- Basic Principles by Jasprit Singh, John Wiley and Sons Inc., 2001
6. Semiconductor Devices- Physics and Technology, by S. M. Sze and M.K. Lee, John Wiley & Sons,3rd Edition, 2012.
7. Fundamental of Modern VLSI devices by Yuan Taur and Tak H. Ning, Cambridge University press, 2nd Edition, 1998.

VL5102 **Analog VLSI Circuits**

L-T-P: 3-0-0 **Credit: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Basic MOSFET device, characteristics, second order effects, MOS device model.	4
2.	**Amplifiers:** Low frequency and high frequency operation of single stage amplifier and differential amplifier **(i) Single stage amplifiers:** common source (CS), source follower, common gate stage, cascade stage with different load; **(ii) Differential Amplifiers:** Basic differential operation, common mode response, Current mirror, differential amplifier with current mirror load.	6
3.	**Noise analysis:** Statistical characteristic of noise, thermal noise, Flicker noise, representation noise in circuits.	3
4.	**Operational amplifier:** one stage OPAMP, two stage OPAMP, gain boosting, common mode feedback, slew rate, power supply rejection.	3
5.	**Bandgap references:** Supply independent biasing, temperature independent references, PTAT and CTAT current generation.	4
6.	**Switched capacitor circuits:** Sampling switches, switched capacitor amplifier, switched capacitor integrator.	3
7.	**Oscillators:** Feedback and Stability, Ring Oscillator, L-C oscillator, Voltage Control oscillator, phase locked loop, Building blocks, locking characteristics and design.	5
8.	**Comparator:** Simple, Switch-based and latch based.	3
9.	**Data Converter:** Characterization of ADC and DAC, ADC and DAC architectures.	3
10.	**Power Management:** LDO and DC-DC Converters	3
11.	**Active Filters:** Design of switch capacitor filer, Design of OTA-C filter.	3
Total number of classes		40

Text Books:

1. Design of Analog CMOS Integrated Circuits by Behzad Razavi , McGraw Hill, 2003
2. CMOS Analog Circuit Design by P.E Allen and Douglas R. Holdberg, Oxford University Press, 2nd edition, 2012.

Reference Books:

1. Analysis and Design of Analog Integrated Circuits by Paul Gray and Robert G Meyer, John Wiley & Sons, 2009.
2. Analog Circuit Design by Johan Huijsing Rudy van Plassche and Willy Sansen, Springer – Science and Business Media, B.V.

VL5103 Digital VLSI Circuits

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Combinational logic design:** Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Ratioed logic-pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles -Domino logic-optimization of Domino logic-NPCMOS-logic style – Voltage scaling.	**10**
2.	**Sequential logic design:** Timing metrics for sequential circuit -latches Vs registers -static latches and registers – Bi-stability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-CMOS register -Dual edge registers-True single phase clocked registers.	**10**
3.	**Semiconductor Memories**: Dynamic Random Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory.	**8**
4.	**CMOS subsystem design:** Data Path Operations: Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Pipeline multiplier array, Booth‟s algorithm, Finite-State Machines.	**6**
5.	**HARDWARE MODELING WITH THE VERILOG HDL :** Hardware Encapsulation –The Verilog Module, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Using Verilog for RTL Synthesis.	**6**
Total number of classes		**40**

Text Books:

1. CMOS VLSI Design –A Circuits and Systems Perspective by Neil H Weste, D Harris and Ayan Banerjee, Pearson, 2012.
2. Digital Integrated Circuits- A Design Perspective by J M Rabaey, Prentice Hall, 3rd Edition, 2012.
3. FPGA based systems, Waney Wolf, Pearson, 1st ed, 2005
4. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital IC-Analysis and Design", Tata McGraw Hill publication.

Reference Books:

1. M.D. CILETTI, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall.
2. M.G. ARNOLD, "Verilog Digital – Computer Design", Prentice-Hall.

VL 5151 Semiconductor Devices and Modelling Lab

L-T-P: 0-0-3 **Credits: 2**

As per syllabus (using Synopsis TCAD and Silvaco TCAD)

VL 5152 Analog VLSI Circuits Lab

L-T-P: 0-0-3 **Credits: 2**

As per syllabus (Using Cadence Tools)

VL 5153 Digital VLSI Circuits Lab

L-T-P: 0-0-3 **Credits: 2**

As per syllabus (Using Cadence , Synopsis ,Mentor Graphics Design automation tools)

Syllabus of Second Semester

VL5201 **VLSI Physical Design**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Algorithmic complexity and optimization problems.	4
2.	**Partitioning:** Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.	4
3.	**Floor planning:** Problem formulation, Classification of floor planning algorithms, Constraint based floor planning, Rectangular dualization.	4
4.	**Pin Assignment:** Problem formulation, Classification of pin assignment algorithms, General and channel pin assignments.	4
5.	**Placement:** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.	4
6.	**Global Routing and Detailed Routing:** Global Routing: Problem formulation, Classification of global routing algorithms, Maze routing algorithms; Detailed Routing: Problem formulation, Classification of routing algorithms, Single layer routing algorithms.	4
7.	**Physical Design Automation of FPGAs:** FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing: Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Physical Design Automation of MCMs: Introduction to MCM Technologies, MCM Physical Design Cycle.	6
8.	**Chip Input and Output Circuits:** ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention, packaging.	4
9.	**On Chip PDN Design:** Noise and Decap Placement.	2
10.	**Lithography Aware Design:** Design for Manufacturability.	4
Total number of classes		40

Text Books:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, Springer International Edition, 3rd Edition, 2005.
2. VLSI Physical Design Automation Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
3. FPGA based systems design, Waney Wolf, Pearson, 1st ed, 2005

References Books:

1. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.

2. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.
3. An Introduction to VLSI Physical Design - Majid Sarrafzadeh, C. K. Wong – " Mc Graw Hill

VL5202 IC Technology

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Integrated Circuits and Planar Process, IC Families, CMOS Process Flow.	2
2.	**Crystal Growth and Wafer Fabrication:** Crystal Structure, Defects in Crystals, Raw materials and Purification, Czochralski and Float-Zone Crystal Growth Methods, Wafer Preparation and Specification, Measurement Methods.	6
3.	**Lithography:** Light Sources, Wafer Exposure Systems, Photoresists, Mask Engineering, Measurement of Mask Features and Defects, Resist Patterns and Etched Features.	4
4.	**Oxidation:** Basic Concepts, Wet and Dry methods, Measurement Methods: Physical, Electrical and Optical, Models and Simulation: Linear and Parabolic, Growth Kinetics, Effect of Temperature, Pressure and Crystal Orientation.	2
5.	**Diffusion:** Dopant Solid Solubility, Fick's Law, Predeposition and drive-in, Gaussian Solution near a Surface, Measurement Methods: SIMS, Spreading Resistance, Sheet Resistance, and Capacitance Voltage.	4
6.	**Ion Implantation:** Role of Crystal Structure, High-Energy Implants, Ultralow Energy Implants, Ion Beam Heating, Measurement Methods, Models: Nuclear Stopping, Electronic Stopping, Damage and annealing.	2
7.	**Deposition:** Manufacturing Methods, CVD, APCVD, LPCVD, PECVD, PVD, Epitaxial Silicon, MBE, MOCVD, Polycrystalline Silicon, dielectrics and metals, Measurement and models.	6
8.	**Etching:** Wet, Plasma Etching, Etching of Various Films, Measurement and Models.	4
9.	**Back-end technology:** Contacts, Interconnects and Vias, Silicide Gates and Source/Drain Regions, IMD Deposition and Planarization, Chemical-Mechanical Polishing, Electro-migration, Measurement methods.	6
10.	**Wafer Processing, Process Variation and DFM**.	3
Total number of classes		**39**

Text Books:

1. Silicon VLSI Technology by James Plummer, M. Deal and P.Griffin, Prentice Hall Electronics and VLSI series, 2009.
2. Semiconductor Devices: Basic Principles, Wiley Student edition, Paperback, 2007, Jasprit Singh
3. VLSI Technology, by S M Sze, McGraw-Hill, 1988.

Reference Books:

1. The Science and Engineering of Microelectronics, by Stephen Campbell, Oxford University Press, 1996
2. VLSI Fabrication Principles by Sorab K Ghandhi, John Wiley and Sons, 2nd Edition, 1994.
3. Microchip Fabrication, McGraw Hill, Sixth edition,
4. Microchip Fabrication by Peter van Zant, McGraw-Hill, 6th edition, 2013.

VL 5203 VLSI Testing and Verification

L-T-P: 3-1-0 **Credits: 4**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction to VLSI Testing:** Role of testing, Verification Vs Testing, Levels of testing, Overheads of testing, Basic testing principle, Ideal tests Vs Real Test.	6
2.	**Fault Modeling:** Defects, Errors and Faults, Functional Vs Structural Testing, Levels of Fault Models, Various types of faults, Fault Coverage, Fault Efficiency, Single Stuckat Fault (Fault Equivalence, Equivalence of Single Stuck at Faults, Fault Collapsing, Fault Dominance, Fault dropping, Check point Theorem), Soft errors.	6
3.	**Logic and Fault Simulation:** Role of simulation in design verification and test evaluation, True value/logic simulation, Algorithms for logic simulation, Fault simulation, Algorithms for fault simulation.	6
4.	**Testability Analysis:** Controllability and Observability, Measures for controllability and observability of combinational circuits, Measures for controllability and observability of sequential circuits; Test Generation for Combinational Circuits; Definition of ATPG, ATPG algorithms for combinational circuits (Roth's D algorithm), and Some applications.	6
5.	**Test Generation for Sequential Circuits:** Classical approach, DFT (Designfor Testability) approach, Time Frame Expansion Method, Complexity of ATPG, and Example of Cyclic Circuit.	6
6.	**Design for Testability:** Design for Testability, Adhoc design, Generic scan based design, Classical scan based design, System level DFT approaches. Built In Self Test (BIST), BIST Techniques, BIST Response Compaction, Circular BIST, Overview of Memory BIST.	6
7.	**Recent trends in Testing and Diagnosis:** Machine learning approaches	4
8.	Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification, Mixed signal design verification (System Verilog, Verilog AMS).	5
9.	Basics of equivalence checking and model checking. Hardware emulation.	5
Total number of classes		**50**

TEXT BOOKS

1. A Roadmap for formal property verification, Pallab Das Gupta, Springer, 1st ed, 2006 with NPTEL lectures.

2. Essentials of electronic testing for digital, memory and mixed signal VLSI circuits, M L Bushnell and V D Agarwal, Springer, 1st ed, 2002

REFERENCE BOOKS

1. Testing and Diagnosis of VLSI and ULSI, F. Lombardi, M.G. Sami, Springer, 1988.

Syllabus of Electives

VL5104/1 Advanced Systems Architecture

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Overview of von Neumann architecture:** CISC and RISC processors, Instruction set architecture; Architecture, Measuring and reporting performance, Data Path Design.	8
2.	**Pipelining:** Basic concepts of pipelining, data hazards, control hazards, and structural hazards; Techniques for overcoming or reducing the effects of various hazards.	6
3.	**Hierarchical Memory Technology:** Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.	8
4.	**Instruction-level parallelism:** Concepts of instruction-level parallelism (ILP), Techniques for increasing ILP; Superscalar, superpipelined and VLIW processor architectures; Vector and symbolic processors; Case studies of contemporary microprocessors.	8
5.	**Multiprocessor Architecture:** Taxonomy of parallel architectures; Centralized shared-memory architecture, synchronization, memory consistency, interconnection networks; Distributed shared-memory architecture, Cluster computers. Multi-core architectures.	6
Total number of classes		**36**

TEXT BOOKS

1. Computer Architecture: A quantitative approach – John L. Hennessy, David A. Patterson – Morgan Kaufmann
2. Computer organization and Architecture : Designing for performance William Stallings – Pearson
3. Advanced Computer Architecture : Parallelism, Scalability and programmability Kai Hwang, Naresh Jotwani – McGraw Hill, 2008

REFERENCE BOOKS

1. Computer Organization and design : The Hardware/Software Interface, David A. Patterson, John L. Hennessy -Morgan Kaufmann, Year: 2004

VL5104/2 Embedded Systems and IoT

L-T-P:3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Features, Design metrics, Design flow.	2
2.	**Microcontroller Systems:** ARM Instruction set architecture, ARM pipeline, THUMB instructions, Exceptions in ARM, Raspberry Pi, Arduino based system design (drone based applications).	5
3.	**Digital Signal Processors:** Architecture, Data access features, Computation features, Accuracy, C6000 family of DSP.	4
4.	**Field Programmable Gate Arrays:** Field programmable devices, Programmability, Logic block variations, Design flow, Modern FPGAs, Concept of soft and hard IP.	5
5.	**Interfacing:** Requirements, SPI, IIC, RS232-C family, USB, IrDA, CAN, Bluetooth, PCI	7
6.	**Real-time System Design:** Task classification, Periodicity, Task scheduling, scheduling algorithms, Resource sharing, Commercial RTOS.	6
7.	**Hardware-Software Codesign:** Introduction to specification, partitioning and co-simulation.	3
8.	**IoT Systems:** Overview of IoT systems, wireless sensor network applications, IoT in Healthcare, automotive and IIoT, Smart Grid.	8
Total number of classes		**40**

Text Books:

1. Embedded System Design, by S. Chattopadhyay, 2nd Edition, 2014.
2. Embedded System Design: A Unified Hardware/Software Introduction, Frank Vahid, Tony D Givargis Wiley,2002.

Reference Books:

1. Embedded System Design, P. Marwedel, 2003
2. Arnold Berger, “Embedded system design” - CMP books

VL5104/3 **Nano and Molecular Electronics**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Nanotechnology and Nanoelectronics; Moore's Law; Review of Semiconductor Electronics: Maxwell's Equation, Poisson Equation, Continuity Equations, carrier concentration, Carrier Transport, Drift and diffusion; basics of molecular electronics.	**4**
2.	**Basics of Quantum Mechanics:** Photoelectric effect; Wave nature of particles and wave-particle duality; Compton Effect; Uncertainty Principle; Schrodinger's equations and its applications; Wave function and postulates; Pauli-exclusion principle; Quantum dots, wires, and wells; Transport in quantum structures; Optoelectronic property.	**14**
3.	**Nanoelectronic Devices:** Overview of MOS and MOSFET; CMOS Scaling and shrink down approaches; FINFET; Tunnel FET; Junctionless Transistor; Single electron transistors; Nanowire MOSFET, GAA FET.	**10**
4.	**Molecular Electronics:** Need of molecular electronics and atoms-up approach; Strategies of electronic development; Molecular bonding and hybridization; Molecules as electronic devices; Carbon molecules & electronics; Pentacene; Transport in molecular electronics; Graphene devices; Carbon nanotube electronics; CNT FET.	**12**
Total number of classes		**40**

TEXT BOOKS

1. C.P. Poole Jr. and F.J. Owens, Introduction to Nanotechnology, Wiley, 2003.
2. D.A. Neamen, Semiconductor Physics & Devices, TMH, 2003.
3. Ashcroft and Mermin, Solid State Physics, Thomson Press (India) Ltd, 2003.
4. G.W. Hanson, Fundamentals of Nanoelectronics, Pearson, 2009.
5. M.C. Petty, Molecular Electronics: From Principles to Practice, Wiley, 2007.

REFERENCE BOOKS

1. C. Kittel, Introduction to solid state physics, Wiley, New York, 1976.
2. K. Iniewski, Nanoelectronics: nanowires, molecular electronics, and nanodevices, McGraw Hill, New York, 2011.
3. K. Sienicki, Molecular Electronics and Molecular Electronic Devices, CRC Press, 1994.
4. S.M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981.
5. J.H. Davies, The Physics of Low-Dimensional Semiconductors, Cambridge University Press, 1998.
6. R.F. Pierrett, Semiconductor Device Fundamentals, Pearson, 2006.
7. B.G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson, 2008.

VLSI5104/4 **Hardware Security**

L-T-P: 3-0-0 **Credits: 3**

Course Outline

This course will focus on the importance of addressing different security threats on modern hardware design, manufacturing, installation, and operating practices. In particular, the threats would be shown to be relevant at scales ranging from a single user to an entire nation's public infrastructure. Through theoretical analyses and relevant practical world case studies, the threats would demonstrate, and then state-of-the-art defence techniques would be described. The course would borrow concepts from diverse fields of study such as cryptography, hardware design, circuit testing, algorithms, and machine learning.

Sl. No.	Module name and topic	No. of classes
1.	Overview of Different Issues of Hardware Security	2
2.	**Preliminaries:** Algebra of Finite Fields, Basics of the Mathematical Theory of Public Key Cryptography, Basics of Digital Design on Field-programmable Gate Array (FPGA), Classification using Support Vector Machines (SVMs).	5
3.	**Useful Hardware Security Primitives:** Cryptographic Hardware and their Implementation, Optimization of Cryptographic Hardware on FPGA, Physically Unclonable Functions (PUFs), PUF Implementations, PUF Quality Evaluation, Design Techniques to Increase PUF Response Quality.	6
4.	**Side-channel Attacks on Cryptographic Hardware:** Basic Idea, Current-measurement based Side-channel Attacks (Case Study: Kochers Attack on DES), Design Techniques to Prevent Side-channel Attacks, Improved Side-channel Attack Algorithms (Template Attack, etc.), Cache Attacks.	6
5.	**Testability and Verification of Cryptographic Hardware:** Fault-tolerance of Cryptographic Hardware, Fault Attacks, Verification of Finite-field Arithmetic Circuits.	5
6.	**Modern IC Design and Manufacturing Practices and Their Implications:** Hardware Intellectual Property (IP) Piracy and IC Piracy, Design Techniques to Prevent IP and IC Piracy, Using PUFs to prevent Hardware Piracy, Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs, Genetic Programming based Modeling of Ring Oscillator PUF).	8
7.	**Hardware Trojans:** Hardware Trojan Nomenclature and Operating Modes, Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans, Logic Testing and Side-channel Analysis based Techniques for Trojan Detection, Techniques to Increase Testing Sensitivity Infrastructure Security: Impact of Hardware Security Compromise on Public Infrastructure, Defence Techniques (Case Study: Smart-Grid Security).	8
Total number of classes		**40**

Text Books:

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press.

Reference Books:

1. Ahmad-Reza Sadeghi and David Naccache (eds.): Towards Hardware-intrinsic Security: Theory and Practice, Springer.
2. Ted Huffmire et al: Handbook of FPGA Design Security, Springer.
3. Stefan Mangard, Elisabeth Oswald, Thomas Popp: Power analysis attacks - revealing the secrets of smart cards. Springer 2007.
4. Doug Stinson, Cryptography Theory and Practice, CRC Press.

VLSI5104/5 VLSI Interconnects

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	Introduction to VLSI interconnects classification, Cu Interconnect, Technological trends, Interconnect scaling, Typical interconnect structure, Electromigration phenomenon, Signal transmission on interconnects, On-chip Interconnects, Package level interconnections.	5
2.	Extraction of interconnect parameters, Physics of interconnects in VLSI, physical foundations for circuit models of VLSI interconnects, Interconnect resistance, capacitance, inductance modelling, Extended Miller effect, Alternatives for extraction. Modelling interconnect drivers. Loss and Lossless transmission line model, Switch-level RC model. T and π network interconnect model. Effective capacitance modelling. Modelling interconnect wires. General interconnect network. An RC tree. The transfer function. Convolution of input and impulse response. Moments of the transfer function. Impulse and step response of RC tree. Elmore delay. Response of single RC. Elmore delay of 2-stage RC. RC-tree. Step response of lumped vs. distributed RC line. Sample RLC network. Modified node analysis equations.	15
3.	Active and Passive interconnections, Multilevel and multilayer interconnections, Propagation delays, Crosstalk effects in digital circuits, spurious signals, crosstalk induced delay, energy dissipation due to crosstalk, crosstalk effects in logic VLSI circuits.	8
4.	Techniques for avoiding interconnection noise, noise detection problem, brief introduction to the testing of logic circuits, Crosstalk configuration, DC noise margins, Crosstalk-induced spurious signal detection, Reasons for high delay uncertainty, switch factor modelling of delay uncertainty, Buffer insertion for noise; Routing topology generation for speed optimization, Width optimization based on separability /monotonicity properties. Introduction to emerging interconnects (CNT, Graphene, optical interconnects and so on.)	12
Total number of classes		**40**

Text Books:

1. Grabinski, Hartmut, "Interconnects in VLSI Design", 1st Edition, Springer, 2000.
2. C-K. Cheng, J. Lillis, S. Lin, N. H. Chang. Interconnect Analysis and Synthesis J. Wiley, 2000.
3. M. Celik, L. Pillegi, A. Odabasioglu. IC Interconnect Analysis. Kluwer, 2002.

Reference Books:

1. A. B. Kahng, G. Robins. On Optimal Interconnections for VLSI. Kluwer, 1995.
2. Moll, Francesc, Roca, Miquel, "Interconnection Noise in VLSI Circuits", 1st Edition, Springer, 2004.
3. J. A. Davis, J. D. Meindl. Interconnect Technology and Design for Gigascale Integration. Kluwer, 2003. F. Moll, M. Roca. Interconnection Noise in VLSI Circuits. Kluwer, 2004.

VL5105/1 **MEMS and Microsystems**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Scaling Laws, Why MEMS?**	2
2.	**Microfabrication Techniques:** Bulk micro machining, surface micro machining and LIGA processes.	6
3.	**MEMS based inertial sensors:** Accelerometer; piezoresistive and capacitive.	6
4.	**MEMS based gyro and tilt sensors**	2
5.	**MEMS based pressure sensor: (Type Pressure Monitoring System)**	2
6.	**Electrostatic actuation:** study of electrostatically actuated micro-machined cantilever beam: Free natural mode of vibration, resonance analysis, static voltage response, pull in and pull out phenomenon. Dynamic response to time varying electrostatic actuation.	4
7.	**RF MEMS:** RF switch, MEMS based inductor and capacitors, MEMS based varactors and resonators.	6
8.	**Optical MEMS:** MEMS based mirrors, MEMS based optical switch.	2
9.	**Microfluidic and Bio MEMS:** advantages of MEMS based fluidic system.	1
10.	Micro pump and Micro valve, Micro nozzle and thrusters, micro needle, micro cantilever based bio sensors, lab on a chip	5
11.	**MEMS based interfacing electronics:** variable gain instrumentation amplifier and wireless integrated micro sensors	4
Total number of classes		40

Text Books

1. Analysis and design principles of MEMS devices by M.-H. Bao,
2. Microsystem Design by Stephen D. Senturia, Kluwer Academic Publishers, 2001.
3. Micro and Smart system by G. K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, Wiley, 2012.
4. Fundamentals of Microfabrication techniques, Marc Madou, CRC Press

VL5105/2 **Quantum Computing**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction to Quantum Computation:** Foundations of quantum theory. States, observables, measurement and unitary evolution.Quantum bits, Bloch sphererepresentation of a qubit, multiple qubits, Qubits versus classical bits, spin-half systems and photon polarisations. Pure and mixed states, density matrices.	**8**
2.	**Background Mathematics and Physics:** Hilber space, Probabilities andmeasurements, entanglement, density operators and correlation, basics ofquantum mechanics, Measurements in bases other than computational basis, Extension to positive operator valued measures and super-operators.Decoherence and master equations. Quantum entanglement and Bell's theorems.Introduction to classical information theory and generalisation to quantum information.	**8**
3.	**Quantum Circuits:** single qubit gates, multiple qubit gates, design of quantumcircuit, Reversible computation.Universal quantum logic gates and circuits,reversible to quantum circuit mapping, Quantum Gate library, Quantum circuit design constraints, Bennett embedding, Nearest Neighbour property, Launder Embedding Constraints.	**8**
4.	**Quantum Algorithms:** Classical computation on quantum computers.Relationship between quantum and classical complexity classes. Deutsch'salgorithm, Deutsch's-Jozsa algorithm, Shor factorization, Grover search, Database search, FFT and prime factorization.	**8**
5.	**Noise and error correction:** Graph states and codes, Quantum error correction,Clifford +Tgroup,fault-tolerant computation.Physical implementations of quantum computers.	**8**
Total number of classes		**40**

Text Books:

1. Nielsen M. A., **Quantum Computation and Quantum Information**, Cambridge University Press.
2. Benenti G., Casati G. and Strini G., **Principles of Quantum Computation and Information**, Vol. I: Basic Concepts, Vol II: Basic Tools and Special Topics, World Scientific.
3. Pittenger A. O., **An Introduction to Quantum Computing Algorithms** 2000.
4. Robert Wille, Rolf Drechsler- Towards a Design Flow for Reversible Logic - 2010 (Springer)

VL5105/3 **Logic Synthesis and Verification**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Overview of the VLSI design flow.**	1
2.	Register-Transfer Level (RTL) Behavioural, Dataflow and Structural synthesis.	2
3.	Hardware modeling principles and hardware description using the VHDL language.	6
4.	Hardware modeling principles and hardware description using the Verilog language.	6
5.	**2-Level Logic Synthesis (Exact & Heuristic Two-Level Logic Minimization):** SOP & POS forms: Costs & Characteristics, Implicants, Cubes and Covers, Quine-McCluskey Method, Minimum Cover via Unate Covering, Branch-and-Bound Methods, The ESPRESSO Minimizer	5
6.	Sequential logic synthesis and state minimization using Finite state Machine (FSM) encoding algorithm**.**	3
7.	**Retiming of sequential circuit synthesis.**	3
8.	**Technology mapping.**	3
9.	**Multi-level Logic synthesis:** SIS, ABC, BDD.	3
10.	**High-level Synthesis (HLS):** DAG scheduling, Register allocation and binding, Datapath and controller design.	3
11.	**Verification:** Introduction to formal methods for verification, BDD, Introduction and construction, OBDD, Operations on OBDD, OBDD for sequential circuits.	5
Total number of classes		**40**

Text Books:

1. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
2. Rudiger Ebendt, Gorschwin Fey, Rolf Drechsler. Advanced BDD Optimization, 2005.

Reference Books:

1. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.
2. Douglas L. Perry, VHDL : Programming By Example 4th Edition, TMH.
3. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
4. Mano, M. Morris, "Digital Design", 3rd Edition, Prentice Hall PTR, 2001
5. Thomas H. Cormen, Clifford Stein, Ronald L. Rivest, Charles E. Leiserson, "Introduction to Algorithms", 2nd Edition, McGraw-Hill Higher Education, 2001.
6. Gary D. Hachtel and Fabio Somenzi, Logic Synthesis and Verification Algorithms. Springer.

VL5204/1 **Low Power Design**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Low power and its applications; Algorithmic, Architectural, Gate and Physical Level power reduction approaches.	6
2.	**Sources of Power Dissipation:** Dynamic Power Dissipation: Short Circuit Power, Switching Power, Gliching Power; Static Power Dissipation, Degrees of Freedom.	8
3.	**Supply Voltage Scaling Approaches:** Device feature size scaling, Multi-Vdd Circuits, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management.	8
4.	**Switched Capacitance Minimization Approaches:** Hardware Software Tradeoffs, Bus Encoding Two's complements verses Sign Magnitude, Clock Gating.	8
5.	**Leakage Power minimization Approaches:** Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS).	6
6.	**Low Power Design Examples:** Memory, Arithmetic circuits.	4
Total number of classes		**40**

Text Books:

1. Low Power VLSI CMOS Circuit Design, by A. Bellamour, and M. I. Elmasry, Springer Science + Business Media, 2012.
2. Low Power Design Essentials (Integrated Circuits and Systems), by Jan Rabaey, Springer, 2009.

Reference Books:

1. Principles of CMOS VLSI Design, by Neil H. E. Weste and K. Eshraghian, Addison Wesley (Indian reprint).
2. CMOS Digital Integrated Circuits, by Sung Mo Kang, Yusuf Leblebici,Tata McGraw Hill.
3. Low Power Digital CMOS Design, by Anantha P. Chandrakasan and Robert W. Brodersen, Kluwer Academic Publishers, 1995.
4. Low Power CMOS VLSI circuit design by Kaushik Roy, Sharat C. Prasad, John Willy & Sons, 2009.

VL5204/2 **Mixed signal circuit design**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Signals, Filters and Tools: Sinusoidal Signals, Comb Filters, Representing Signals, Sampling and Aliasing.	4
2.	**Filters:** Continuous-time filters, Discrete-time filters, Analog and discrete-time signal processing, Analog integrated continuous-time and discrete-time (switched-capacitor) filters.	6
3.	**Digital Converters:** Basics of Analog to digital converters (ADC), Basics of Digital to analog converters (DAC), DACs, Successive approximation ADCs, Dual slope ADCs, High-speed ADCs: flash ADC, pipeline ADC and related architectures, High-resolution ADCs: delta-sigma converters.	8
4.	**Phase locked loops:** Phase Detector Voltage Controller Oscillator, Loop Filter: XOR DPLL, PFD DPLL, System Concerns: Clock Recovery From NRZ Data, Delay-Locked Loops.	6
5.	**VLSI Layout:** Chip Layout: Regularity, Standard Cell Examples, Power and Ground Considerations, Layout Steps by Dean Moriarty: Planning and Stick Diagrams, Device Placement, Polish, Standard cells Versus Full-Custom Layout.	8
6.	**Interconnects:** Basics, application, RC delay and its model.	6
Total number of classes		**38**

Text Books

1. CMOS mixed-signal circuit design by R. Jacob Baker, Wiley India, IEEE press, 2008.

Reference Books:

1. Design of analog CMOS integrated circuits by Behzad Razavi, McGraw-Hill, 2003.
2. CMOS circuit design, layout and simulation by R. Jacob Baker, Revised second edition, IEEE press, 2008.
3. CMOS Integrated ADCs and DACs by Rudy V. dePlassche, Springer (Indian edition), 2005.
4. Electronic Filter Design Handbook by Arthur B. Williams, McGraw-Hill, 1981.
5. Design of analog filters by R. Schauman, Prentice-Hall 1990.

VL 5204/3 **RF IC design**

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L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction RF and Wireless Technology**: Complexity, design and applications. Choice of Technology.	2
2.	**Basic concepts in RF Design:** Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion	4
3.	**Analog and Digital Modulation for RF circuits:** Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.	10
4.	**Basic blocks in RF systems and their VLSI implementation:** Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations.	6
5.	**Oscillators:** Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonator-less VCO design. Quadrature and single-sideband generators.	6
6.	**Radio Frequency Synthesizers:** PLLS, design of integer-N RF frequency synthesizer and frequency dividers.	5
7.	**Design issues in integrated RF filters:** Some discussion on available CAD tools for RF VLSI designs; Prerequisite: (Analog VLSI Design).	4
8.	**RF power amplifier and linearization techniques:** Classification of power amplifiers, design of class AB and class E amplifier, various techniques of linearization in cartesian mode.	3
Total number of classes		40

Text Books

1. RF Microelectronics by B Razavi, Prentice-Hall PTR, 1998.
2. The Design of CMOS Radio-Frequency Integrated Circuits, by T H Lee, Press, 1998.
3. Power Amplifier by Cripp.

Reference Books:

1. CMOS Circuit Design, Layout and Simulation, by R J Baker, H W Li, and D.E. Boyce, Prentice-Hall, 1998.
2. Mixed Analog and Digital VLSI Devices and Technology by Y P Tsividis, McGraw Hill, 1996.

VL 5204/4 **SoC Design and Testing**

L-T-P: 3-0-0 **Credits 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction to the System Approach:** System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SoC Design, System Architecture and Complexity.	6
2.	**Hardware/software co-design:** partitioning, real-time scheduling, hardware acceleration	4
3.	**Memory Design for SoC -** Overview of SoC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SoC Memory System, Models of Simple Processor – memory interaction.	6
4.	**Interconnect Customization and Configuration:** Inter Connect Architectures, Bus: Basic Architectures, SoC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SoC Customization.	6
5.	**Transaction-Level Modeling (TLM), Electronic System-Level (ESL) languages:** SystemC.	5
6.	SoC and IP integration, verification and test.	6
7.	**Network on Chips:** Introduction, Components, NOC Layers, Topologies, Routing.	4
8.	3D IC : Synthesis ,Power management and test issues.	3
Total number of classes		**40**

Text Books

1. Design of System on a Chip: Devices and Components, Ricardo Reis, 1st Edition, 2004, Springer
2. System on Chip Verification – Methodologies and Techniques, Prakash Rashinkar, Peter Paterson and Leena Singh L, "2001, Kluwer Academic Publishers.
3. Computer System Design System-on-Chip, Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.

References

1. Multiprocessor Systems-on-Chips, A. Jerraya and W. Wolf, eds., Morgan Kaufmann, 2004
2. ARM System on Chip Architecture ,Steve Furber, "2nd Edition, 2000, Addison Wesley Professional.
3. Network on Chip: The next generation System on Chip integration,Santanu Kundu, Santanu Chattopadhyay ,CRC Press, Year: 2014

VL 5204/5 **Emerging Technologies**

L-T-P: 3-0-0 **Credits 3**

Sl. No.	Module name and topic	No. of classes
1.	**Microfluidic biochips**: Introduction to Microfluidics, Lab on Chip devices, Flow based and digital microfluidic biochips, Biochip actuation techniques, Biochip application, Design Automation techniques for DMFBs, Chip level design for biochips, Paper based and MEDA based biochips	8
2.	**Optical circuits:** Fundamentals of optical switching and its applications, MZI and its application as an optical switch, reversibility and reversible circuit using MZI,optical logic gates	8
3.	**Memristors:** Introduction to Memristor -An overview to the Memristor technology and non-Von Neumann architecture. Memristive-Devices- Types of Memristor – RRAM, PCM, STTMRAM. Utility of using RRAM for in-memory computations Computational models for RRAM- Introduction to VTEAM model and, Stanford memristor-models. Logic design techniques using memristor- IMPLY, MAGIC, MRL, MTL Logic synthesis methodologies inside Memristive-memory- Introduction to logic synthesis tools – ABC, SIMPLE MAGIC. Future possibilities-A huge possibility for energy efficient and, performance efficient non-Von Neumann machines of future	7
4.	**CNT/GNR:** Graphene Basics, Introduction to Carbon nanotube (CNT) and Graphene nanoribbobn, Single-Wall (SW) and Multi-Wall (MW) CNT, CNT based FET and interconnect, Single layer (SL) and Multi layer (ML) GNR, GNR based FET and interconnect. Introduction to modelling techniques and performance analysis of CNT and GNR based device and interconnect for high speed power aware VLSI design.	10
5.	**Reversible logic:** fundamentals of rveresible logic and gates,Reversible logic synthesis and design of reversible circuits	7
	Total number of classes	40

Text Books

1. Digital Microfluidic Biochips:Design Automation and Optimization, Krishnendu Chakrabarty,Tao Xu – CRC Press,2010
2. Digital Microfluidic Biochips: Synthesis,Testing and reconfigurable Techniques, Krishnendu Chakrabarty ,Fei Su – CRC Press/Taylor and Francis,2007
3. Carbon Nanotube and Graphene Nanoribbon Interconnects, Debaprasad Das, Hafizur Rahaman, 1/e CRC Press.
4. Memristors and Memristive systems R. Stanley Williams (auth.), Ronald Tetzlaff (eds.) Publisher: Springer-Verlag New York, Year: 2014
5. Memristor networks , Andrew Adamtzky,Leon Chua, World Scientific Press
6. Robert Wille, Rolf Drechsler- Towards a Design Flow for Reversible Logic - 2010 (Springer)

VL 5205/1 **VLSI Architecture for DSP**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Introduction to DSP systems, DSP application demand and scaled CMOS technologies, representation of DSP algorithms, DFT and FFT.	3
2.	**Iteration bound:** Introduction, data flow graph representations, loop bound and iteration bound, algorithms for computing iteration bound.	4
3.	**Pipelining and parallel processing:** Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.	5
4.	**Retiming:** Introduction, properties, solving systems of inequalities, retiming techniques.	6
5.	**Unfolding:** Introduction, algorithm for unfolding, properties, critical path, unfolding and retiming, applications.	6
6.	**Folding:** Introduction, folding transformation, register minimization techniques, register minimization in folded architectures.	6
7.	**Systolic Architecture Design:** Introduction, systolic array design methodology, FIR systolic arrays, scheduling vector, matrix multiplication and 2D systolic array design.	4
8.	**Bit level arithmetic architectures:** Introduction, parallel multipliers, bit serial multipliers, bit serial filter design and implementation, canonic signed digit arithmetic, distributed arithmetic.	4
9.	**Redundant Arithmetic:** Introduction, Redundant number representation, carry free radix-2 additions and subtractions, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architecture, data format conversion.	4
Total number of classes		**42**

Text Books

1. VLSI digital signal processing systems by K K Parhi, John Wiley & Sons, 1999.

Reference Books:

1. DSP with FPGA by U. Meyer-Baese, Springer, 2004

VL5205/2 **FPGA system design**

L-T-P: 3-0-0 **Credits: 3**

Sl. No.	Module name and topic	No. of classes
1.	**Introduction:** Different kinds of programmable logic devices: Field Programmable Gate Array (FPGA), Programmable Logic Device (PLD), FPGA manufacturers (Xilinx, Altera, Actel, Lattice Semiconductor, Atmel). FPGA applications. Adjoining devices. Instruments and software.	10
2.	**The Structure of FPGA:** FPGA general description. Different kinds of FPGA packages. FPGA architecture. Internal hard modules of FPGA (CLB, Block RAM, DCM), their meanings and usage. Different kinds of I/O modules, their usage and configuration.	10
3.	**FPGA Design Flow:** Architecture design. Project design using Verilog Hardware Description Language (HDL). Defining testing methodology and testbench design. RTL simulation, synthesizing, implementation, gate level simulation of design. Reusing of internal hard modules during design and implementation.	10
4.	**Testing Methodology:** Functional and gate level testing. SDF file description and usage.	5
5.	**FPGA Configuration:** Different types of FPGA configuration files. Generation of configuration file and its loading into FPGA.	5
Total number of classes		40

Text books:

1. Scott Hauckand Andre Dehon. Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation (Systems on Silicon Book 1)

Reference Books:

1. D. Amos, Au. Lesea, R. Richter. "FPGA-Based Prototyping Methodology Manual", 2011
2. D. Vega. FPGA 133 Success Secrets - 133 Most Asked Questions on FPGA - What You Need to Know. Emereo Publishing, 2014
3. V. Sklyarov, L. Skliarova, A. Barkalov, L. Titarenko. Synthesis and Optimization of FPGA-Based Systems. Springer; 2014
4. P. Chu Pong, "FPGA Prototyping By Verilog Examples", Xilinx Spartan, 3rd version, 2008
5. High-performance ASIC Prototyping Systems (HAPS) Datasheets
6. Spartan-3A/3AN FPGA Starter Kit Board User Guide, 2010
7. PLD, FPGA Datasheets.